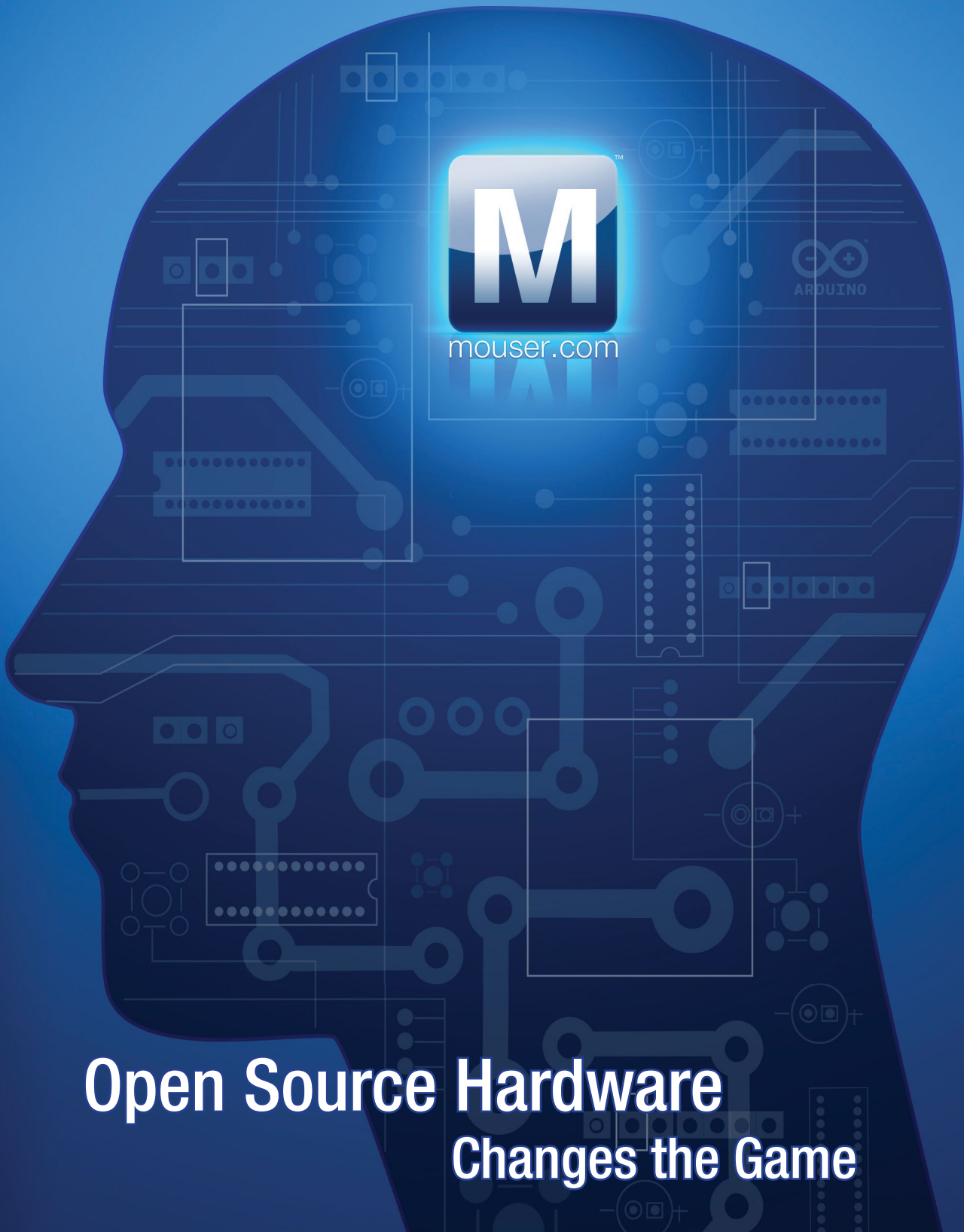


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Open Source Hardware Changes the Game

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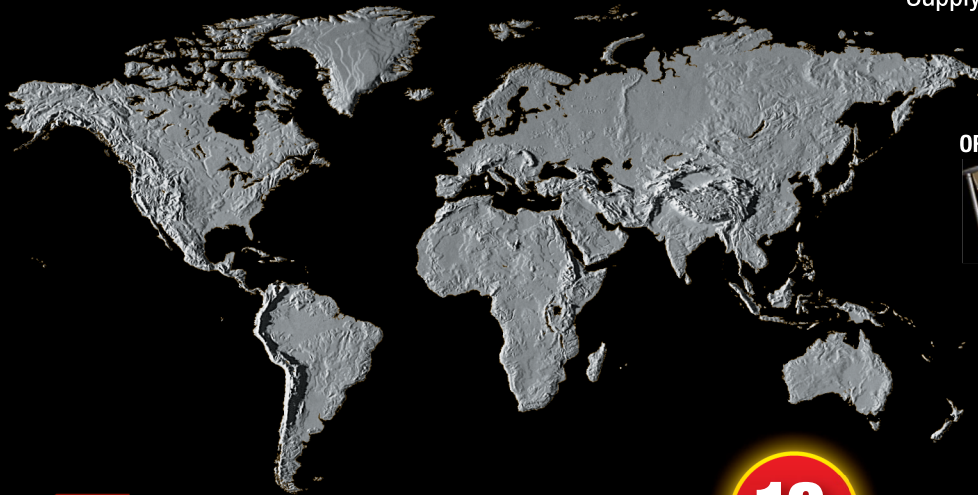


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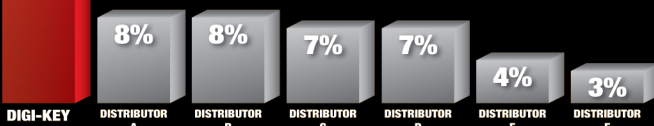
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'BEST OF CLASS' FOR BROADEST OVERALL PRODUCT SELECTION?

Source: 2012 Design Engineer and Supplier Interface Study, Hearst Business Media, Electronics Group, North America, May 2012



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OPINION

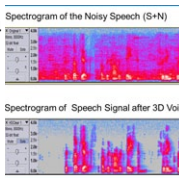
- 4 Uncommon Market: Smart city boost for the UK
- 50 Last Word: Bench-top cleaning - be careful what you ask for

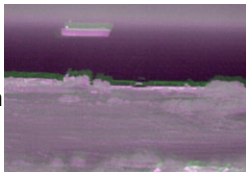
NEWS & TECHNOLOGY


- 6 Chip engineers prepare for 450mm wafer transition
- 8 Open source hardware changes the game
Embedded technology is facilitated by the standardization of operating systems so that applications can run on any platform that supports the standard.
- 10 So-Light research project gives OLED technology a boost
Eleven German OLED companies and research institutions successfully completed the So-Light project which addressed the complete value chain, from primary materials to lighting applications. 
- 10 « Coil on Module » chip package could help ramp-up adoption of dual interface smart cards
- 12 Flash Forward at the leading edge?
Sandisk, a leading supplier of data storage products, has announced it intends to begin the transition of its flash products to 1Y-nm generation semiconductors in the third quarter of 2013.
- 12 Nano-positioning system relies on magnetic levitation, achieves 10nm resolution 
- 14 Taking a new direction with analog
With the introduction of the MCP19111 single chip solution, Microchip is claiming the world's first digitally enhanced power analog controller. 

DESIGN & PRODUCTS

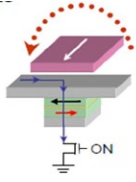
SPECIAL FOCUS: - AUDIO & VIDEO ELECTRONICS

- 16 3D noise cancellation makes voice control significantly more reliable
Voice quality is becoming a hot issue due to the recent rise of voice control interfaces for tablets, computers, Smart TVs and other consumer electronics. 

- 20 Designing low-power video image stabilisation IP for FPGAs
Image stabilisation is an important capability for many electro-optic sensors, where an operator or user is required to view the output imagery. 

- 23 Testing HDMI and MHL successfully
Manufacturers test these interfaces at different stages in the value chain to verify their functionality and compliance with standards. 

- MEMORY & DATA STORAGE

- 29 Bit by Bit, DRAM module testing
- 31 From ROM to Flash for added flexibility
Restrictions of ROM-Based technology require new memory concepts. Until now, data were saved on a chip card with security controllers based on ROM and EEPROM memory technology.
- 34 Moving from magnetic random access memory to magnetic logic units 
- 36 Hybrid Memory Cube gen 2 on track to support a total cube bandwidth of 160GB/s

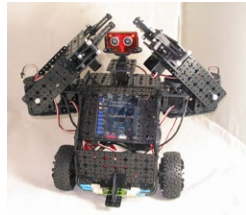
- EMBEDDED ELECTRONICS

- 38 EEMBC to develop Ultra-Low Power microcontroller benchmarks
- 38 Samsung reveals eight-core mobile processor
Samsung Electronics has launched an eight-core ARM-based processor that uses the big-little processing technique announced by ARM Holdings plc in 2011.

- TECHNOLOGY REPORT

- 42 Developing and strengthening 3D IC manufacture in Europe
The European 3D TSV Summit that took place at Grenoble's Minatec campus late February gathered 320 attendees from over 20 countries, a testimony of Grenoble's high tech reputation and France's competitive edge in the field of 3D IC integration. 

READER OFFER

- 46 This month, Multiplo is giving away three Robot Building Kits, worth USD 239 each to design and prototype your own fully functional robots. 

49 DISTRIBUTION CORNER

Smart city boost for the UK

By Nick Flaherty

SMART CITIES ARE a key element of innovation strategy in Europe, and provide key opportunities both for the development of new sensor, monitoring and control technologies but also as potentially huge markets for companies with expertise in these embedded areas.

Cities across the UK have been competing for a key £24m smart city project over the last year, won by Glasgow, Scotland's second largest city. The Future City demonstrator will provide real-time information about traffic and apps to check that buses and trains are on time. The council will also create an app for reporting issues such as potholes and missing bin collections.

Other services promised by the council include linking up the CCTV cameras across the city with its traffic management unit in order to identify traffic incidents faster. It will use analytical software and security cameras to help identify and prevent crime in the city and monitor energy levels to find new ways of providing gas and electricity to poorer areas where fuel poverty is a big issue.

"Glasgow has some quite extreme challenges – it has the lowest life expectancy of any city in the UK for instance – and the hope is that if we bring together energy, transport, public safety and health it will make it more efficient and a better place to live," said Scott Cain, the TSB's project leader for Future Cities, although the project team denied that affluence was a factor in the decision making.

That view was backed up by UK Universities and Science Minister David Willetts. "With more people than ever before living in our cities, they need to be able to provide people with a better quality of life and a thriving economy," he said. "From transport systems to energy use and health, this demonstrator will play a key part in the government's industrial strategy and give real insight into how our cities can be shaped in the future," he added.

Glasgow was the first UK city to win the smart city status from IBM in March 2011, and gained key experience on IT systems and sensors. IBM has been increasing its involvement with smart cities in Europe. Its Dublin facility is the only Smart City research lab and looks at research in water, energy, transportation, city fabric, risk, exascale computing, and marine environments. The lab is comprised from researchers from institutions

such as the Massachusetts Institute of Technology (MIT), the École Polytechnique Fédérale de Lausanne, Cambridge University, the Australian National University, and Trinity College Dublin. The lab is also directed and managed by staff from the IBM Thomas J. Watson Research Center.

However the decision to back Glasgow was a surprise. "Industry expectations have been overturned throughout this competition, and this result, too, will surprise many," said Joe Dignan, Chief analyst for

European Public Sector at market researcher Ovum. Initially, the smart money was on Bristol, Birmingham, Leeds + Bradford or Manchester to scoop the prize, given their level of preparation. However, only Bristol joined the short-list alongside Glasgow, Peterborough and London. Peterborough was considered the wild card, while most felt London had already been given more than its fair share of the public purse in the lead up to the Olympics.

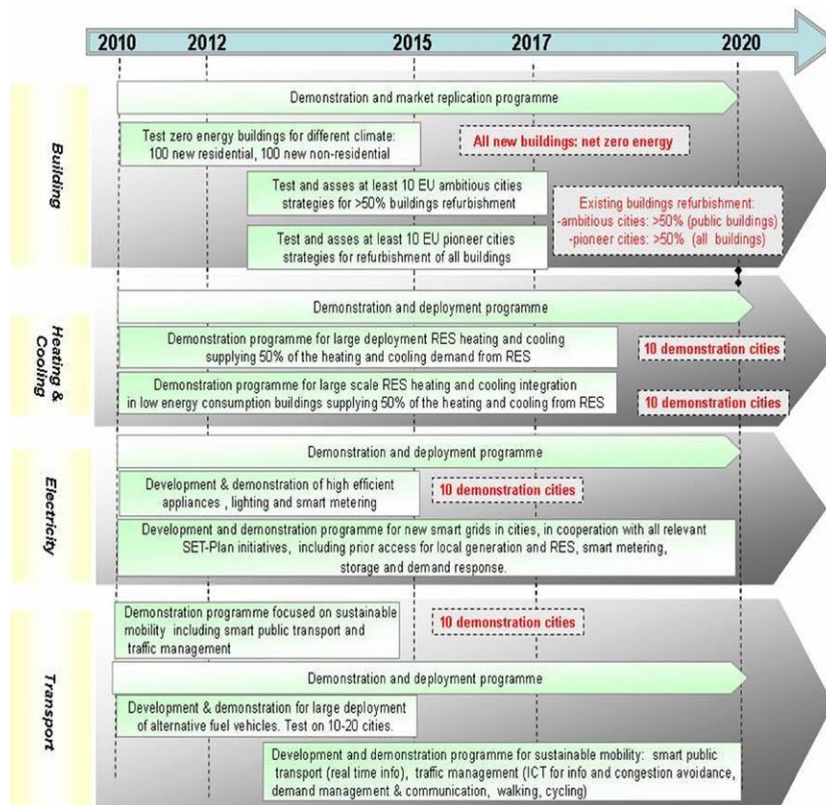
"Glasgow's success reflects a global trend in the development of future cities being presaged by a major global event. Although it was considered the outsider in this race, its preparation for the 2014 Commonwealth Games was the catalyst to get the right people around the table to look

at the performance of the city as a whole," he added. "There is no doubt that the judging process was objective and Glasgow's bid excellent, but one can be sure that Westminster is happy to show its commitment to Scotland at the current time."

While Bristol lost out to Glasgow for the Future City demonstrator project, the TSB judges rated the city's bid very highly, so much so that they have awarded a £3m 'runners-up' prize.

"While there is some disappointment that we did not gain the main prize, Bristol is now the only city in the UK to have won funding from Government to be both a Super Connected City and a Future City," said George Ferguson, the newly elected mayor of Bristol... "Bringing these awards together gives us a pot of nearly £15m with which we can move really quickly to lever-in additional funding and support from business to help deliver our plans."

Bristol's Smart City programme was also launched in March 2011 with funding from the UK Department for Energy and Climate Change and in August 2011 it raised over £300,000 from the EU for two projects as part of its Smart City Programme.



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Chip engineers prepare for 450mm wafer transition

By Christoph Hammerschmidt

AT THE 10TH INNOVATION Forum on Fab Automation in Dresden, participants and presenters discussed technology trends in manufacturing automation. Since this event has been launched by a group of companies which are active in the field of semiconductor manufacturing and is attended in the first place by participants out of this industry segment, it is only natural that the presentations also focused on automation in IC production - especially as the host for this year's forum was chipmaker Globalfoundries.

Although many players in the European semiconductor industry resist the introduction of 450mm wafers, it is inevitable we'll climb this technology step, predicted Malcolm Penn, CEO of market research firm Future Horizons. And despite the horrendous costs circa US\$10 billion and more, such fabs will be cost-effective compared to 300mm fabs. The productivity of this new class of giga-fabs will be boosted by new production concepts which include a high degree of automation. In contrast to the transition to the 300mm node, this time the transition will be properly planned and orchestrated throughout the industry, Penn said. Pioneering this transition are the Albany R&D lab which currently is conducting trials with one-off tools, and the Belgian research institute IMEC whose 450mm clean room is now approved and under construction. Yet unclear is the situation at the wafer supply side. "This is still a kind of bottleneck", Penn said.

While there is no compelling interdependency between geometry node, wafer size and lithography technology, these parameters will "inevitably" be coordinated, the analyst stated. Nevertheless it will take quite a while until the transition is really complete. Penn expects volume production of "real" 450mm wafers not to be launched before 2018, and by this time, the industry will have reached the 8nm node. As a consequence of the competitive pressure generated by the 450mm fabs, existing 300mm production lines will migrate to 'More than Moore' products as already announced by some market players such as Infineon and Texas Instruments. Penn described the 450mm technology as a kind of industrial mass destruction weapon, which will "annihilate" any 300mm-based production with its overwhelming productivity. Still the best chances for the conventional fabs

processing wafers of 300mm or less will be found in the markets for advanced LED products and SiC substrates, the market analyst said. "It is tragic that ST, NXP and Infineon are so unenthusiastic about embracing 450mm" Penn criticized. "This could destroy the whole European microelectronics industry".

Nevertheless, Europe will continue to be a key contributor to the 450mm technology. Namely ASML is about to become the key R&D lithography provider for the world. "Japan seems to have almost given up trying to match ASML", Penn said.

Along with the transition to larger wafers and smaller geometries, the industry is preparing for the introduction of EUV (Extreme Ultra Violet) lithography. Markus Bender, Innovation Engineer for the Advanced Mask Technology Center (AMTC) in Dresden, provided valuable insights into the state of the EUV technology. The AMTC, a joint venture of Globalfoundries and Toppan Photomasks Inc., provides lithography masks for chipmakers across Europe and deals with leading-edge EUV technology.

Nevertheless, there is a number of critical issues. The most important ones are creating a mask yield and deflection inspection review infrastructure, building a reliable long-term light source, and developing high quality photoresists that meets the requirements for ultra-small geometries.

By 2014, the ongoing trend towards smaller geometries will generate the need for a reliable EUV source for the first cost-effective chip production. By this time, 200W of power will be sufficient, Bender said. Over time, the source power needs to be augmented from 500 to 1000W. Since no EUV pellicle is available today, mask protection is another

issue. For this reason, masks need to be cleaned at the point of use which certainly hampers productivity as long as no pellicles are developed. According to Bender, a workaround is the use of dual pods. In addition, the price per mask will be significantly higher than for a conventional lithography mask.

All in all, it remains to be seen if the use of EUV technology eventually will lead to lower prices per transistor compared to conventional processes, Bender said. Nevertheless, EUV will be introduced into commercial production "within the next couple of years", the insider expressed his belief. Actually, this is what the industry has been announcing for many years, but "now it is really about to happen", Bender corroborated.

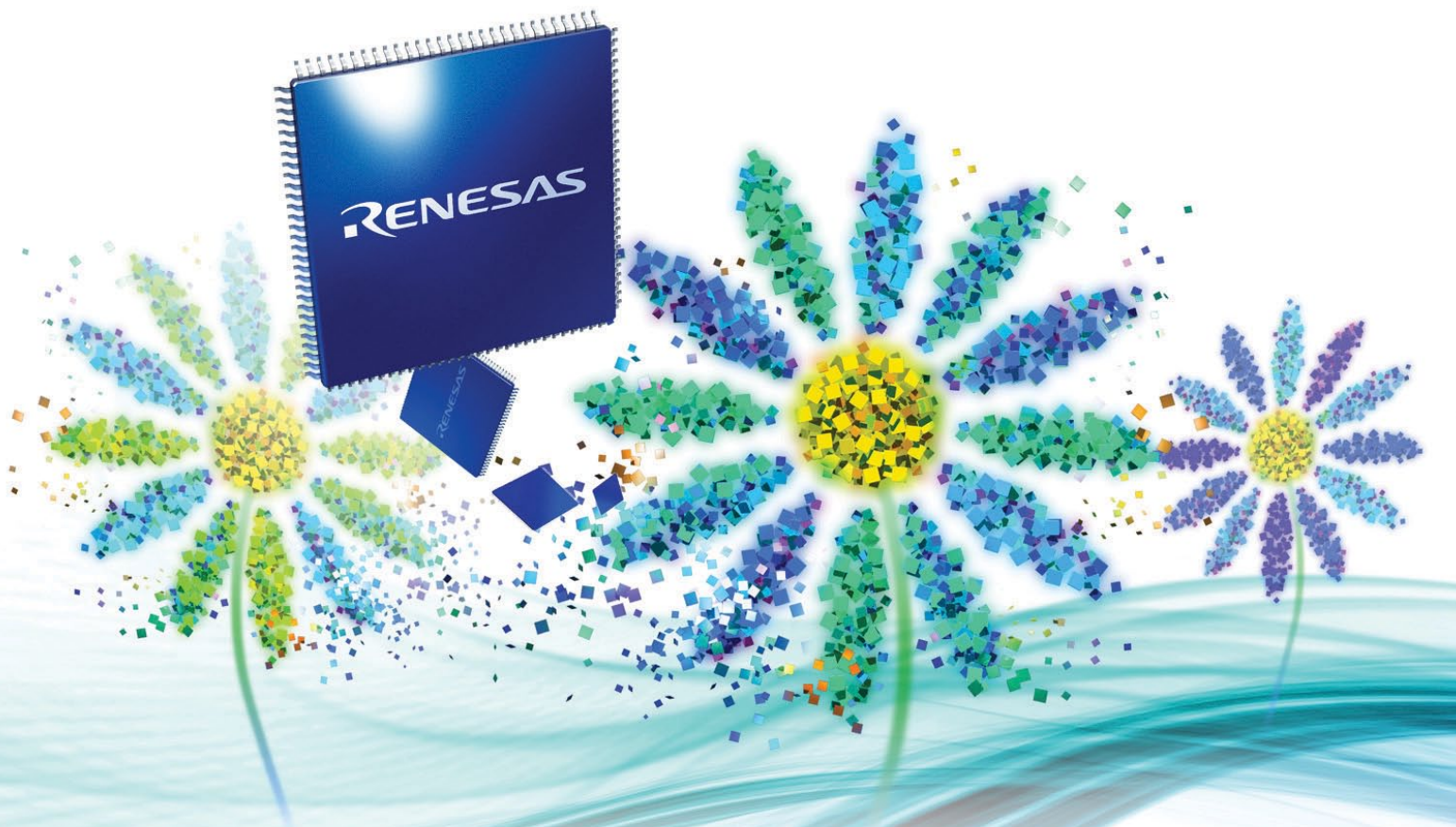


Automation and productivity in semiconductor manufacturing were hot topics at the 10th Innovation Forum in Dresden. Here, a wafer handling robot.

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Open Source Hardware Changes the Game

By Lynnette Reese, Mouser Electronics

EMBEDDED TECHNOLOGY IS facilitated by the standardization of operating systems so that applications can run on any platform that supports the standard. Witness the overwhelming success of the open source software (OSS) movement. For software, it means that source code is free to obtain, use, and revise without payment of any kind to the originators. In return it is expected that the user will credit the original source of the code and perhaps contribute code back to the originating community. Cases in point: Linux enabled Google to build dirt-cheap servers; Java, Perl, and Ruby have become the lingua franca for building Web 2.0 applications; and the free Web-server software Apache enables nearly half of all the world's web sites. OSS can be said to have given birth to the Internet age, making everyone – including those who donated their labor – better off.

Likewise, Open Source Hardware (OSHW) is a potential game changer for the electronics market. Open source hardware (OSHW) is a component or device that has been licensed to allow anyone to examine, duplicate, and modify the hardware as they wish. With open source, you can share and adapt the work freely, and if you choose to sell or distribute it, you can do so under the same license.

Open source hardware is popular with hobbyists, and we may see product development with OSHW by commercial companies increase, as it has with Linux. Linux became a major engine of growth for embedded software once the large players realized that it was royalty-free and that it was legally supportable for their purposes. For instance, early on, the set-top box industry in the United States was under extreme pressure to create low-cost boxes when the cable industry began providing boxes free in order to gain subscribers. Linux was a cost-free operating system to run on the set-top-box platform. Linux is perfect to use on evaluation boards for demonstrating new

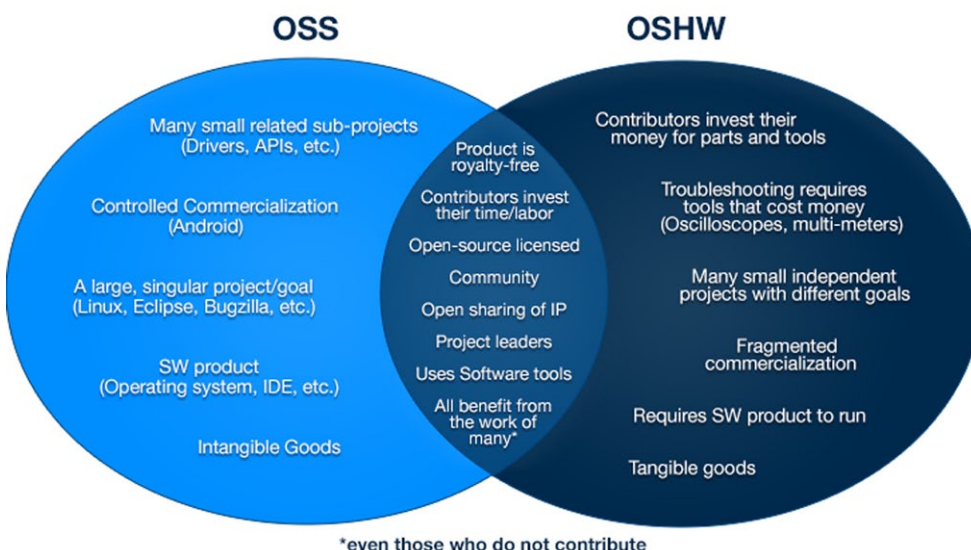
semiconductor processor chips, as well. Development boards to evaluate new technologies and platforms exposed other, customer-companies to embedded Linux. The open source hardware movement will likely mature in a similar manner. It will always hold great appeal for hobbyists and educators because economically speaking, barriers to entry are very low; it can quickly become the platform of choice for start-ups with great ideas and less money to take those ideas to market.

The main difference between OSHW and OSS is that OSS is completely free if you consider using the internet to transfer source code as “free.” OSHW involves cost of the materials. So the real point here is that the hardware IP is what is free. Contributors either make or purchase a platform before they can contribute (Figure 1.) Even so, multiple modifications and additions are uploaded by contributors. For commercial ventures, this can be a real time-to-market advantage, because it allows for fast prototyping and produces a device that may be iteratively tweaked or hacked; the entire design is out in the open. People like to make things and share them in communities because they make friends, earn respect, learn from others, and get feedback on their contributions. There are hundreds of OSHW projects published online today.

As with OSS, sharing with the OSHW community is not only allowed, it's encouraged. One example of OSHW is the Arduino platform where commercial re-use of Arduino designs requires no royalties. Mouser Electronics offers the Arduino line, which supports ARM-based processors, as well as other OSHW lines: the Beagleboard using Texas Instruments' processors, the Pinguino and ChipKit™ with Microchip processors, and the Freescale Olimex, among others. (Figure 2.)

Unlike a free reference design, OSHW typically involves a community of developers that contribute their time and expertise with no expectation of payment for their effort. Some of the best benefits of open source are that many people with varying experience participate, which creates more robust designs, and offers collective intellectual property for free. Integrity, technological intelligence, and the elegance and cleverness in the execution of a solution are all rewarded. And this easier, faster, and cheaper way to design could fundamentally shift the hardware design and manufacturing paradigm.

In supporting the community, Mouser stocks and delivers the newest OSHW offerings. A powerful development board that is difficult to keep on the shelf is the Arduino Due. It's based on the Atmel SAM3X8E ARM® Cortex™-M3 micro-controller running up to 84MHz, providing flexibility and power. This is the first Arduino based on a 32-bit processor and enables new sketches for playing audio from an SD card and a USB Host. Open



Open Source Ecosystems Differ Primarily Due to the Cost of Materials for Contributors

source hardware allows people to quickly create products that solve problems or merely entertain. Standing on the shoulders of other contributors, people can take a short route to translating their ideas into a functioning reality. Arduino is just one example.

Mouser also supplies the BeagleBone developed by BeagleBoard.org and manufactured by Circuit Co. The BeagleBone eliminates barriers with simple development based on the ARM® Cortex™-A8 processor that runs Android 4.0 and Ubuntu software. Open-source Linux developers can easily add peripheral functionality with plug-in boards called “capex” (camera, touch screen, motor control, battery power, and more), enabling rapid product development.

Another solution Mouser carries is from Microchip Technology as the chipKIT™ UNO32 Arduino-Compatible 32-Bit MCU development platform. The environment is based on the original Arduino IDE, and modified to support PIC32 devices while still supporting the original Arduino line. This platform allows hobbyists and students to develop original embedded applications easily and quickly, including motor control, LCD display, wired/wireless communications, LED matrix control, and sensor networks. Other leading OSHW suppliers include Olimex, Pandaboard.org, and SolderCore, using ARM-based processors from Freescale and Texas Instruments.

Open source software regularly complements open source hardware. One commonality between OSS and OSHW is how change is governed. Google’s Android operating system is open source: anyone can take the source code and alter it or use it, with some common sense restrictions. For instance, if your new OSS-based code forks away from the moderated base version, it takes a separate development path and your operating system is no longer built-upon by other open source contributors that maintain the main tree. Your code will eventually be orphaned from any new development that follows unless you work to keep your uncontributed modification up-to-date with every new addition to the main tree of code. Maintaining consistency is critical to Linux because as a mature OSS there are thousands of lines of code to debug. Change occurs rather slowly. Anyone who needs XYZ interface immediately for product development is faced with creating, contributing, and probably maintaining the Linux driver for XYZ interface in perpetuity.

Technology is rather picky in its choice of friends. New code or hardware is useless and gets ignored if it doesn’t play well with other established modules. OSHW is less shareable because it requires physical goods and money as the source, or “tree” to build upon. For these reasons, OSHW is more fragmented; many people buy the boards and build their own project as their only goal. With OSHW, it either works on the base platform or it doesn’t. The maintainers are also the ones who sell the platforms; if your idea isn’t accepted, it is not incorporated into the platform. Arduino has followed the Linux model by establishing proven hardware modules called “shields” that quickly provide technology options, such as Ethernet capability. OSHW and OSS are both governed by technology standards. USB is a very well-defined technology that will not work well

A Comparison of OSHW Boards		
Hardware	Core	Of Note
Arduino Due	Atmel SAM3X MCU based on the 32-bit ARM® Cortex™-M3 running up to 84MHz	New USB Host and Audio sketches. Ideal for high-speed data transfer. Dual FLASH banks, 54 digital I/O, 12 Analog Input, 2 Analog (DAC) outputs, USB. Up to 12 PWM.
Arduino Leonardo	8-bit Atmel ATmega32u4 core running at 16 MHz	Flexible. Single USB cable for communication to the host. 20 digital I/O.
GHI Electronics FEZ Cerbuino Bee Mainboards	STM32 F4 with an ARM® Cortex™-M4 core running at up to 168 MHz	Arduino compatible. Low-cost. MicroSD socket, USB host and device, programmable LED, WiFi, ZigBee, CAN 9AI, 2 AO, 6 PWM, Real time clock, Ethernet.
Olimex OLinuXino-MAXI	Freescale i.MX233 MPU based on the ARM926EJ-S core running at 454MHz	Industrial grade. Integrated graphics controller and analog stereo audio. Ethernet support. 2 USB hosts. No wireless.
Microchip ChipKIT™ Uno32	Microchip PIC32: 32-bit MIPS M4K core running at 80MHz	Arduino-compatible software. Industrial and Automotive-grade. USB host/device/OTG, 2 CAN ports.
Beagleboard.org Beaglebone	TI AM335x Sitara™ MPU based on the ARM® Cortex™ A8 core running at 720MHz	Ethernet, Video, LCD panel, USB host and OTG, no wireless.
Soldercore SC-CPU	TI LM359 Stellaris with an ARM® Cortex™ -M3 core running at 80 MHz	Arduino form-factor, USB OTG and on-board micro-SD Card holder. User programmable: 5 LEDs and 20 GPIO
Pandaboard/ES	TI OMAP4460 with a dual-core ARM Cortex™ A9 MPCore™ with Symmetric Multiprocessing (SMP) at 1GHz each.	Mobile software development platform. USB, LCD, and camera expansion headers. Ethernet, HDMI, DVI, Audio, Bluetooth, 802.11 b/g/n.

A Comparison of Open Source Hardware Development Platforms

with other USB products if the standards are not followed, whether it is hardware or software.

Meanwhile, OSHW is another way to go green. In “the old days” appliances were kept for years and repaired; most user manuals came with a schematic. Nowadays it is often cheaper to buy a new product than to repair it. OSHW changes the game in that a customer can have access to the schematics and help online. As resources become more constrained, repair may be the lower-cost approach again someday. A repaired product does not create waste in a landfill nor require new resources from a foundry. In the future, perhaps only a significant improvement in energy efficiency could trump repair and cause a new purchase.

Whether the reason is to jump-start a new product design, investigate a new technology, or to create one of the many DIY embedded projects published online, Mouser.com has everything you need to embark on a voyage of discovery into open source hardware. Since the invention of electricity, DIY hardware projects have been advertised for purchase in the final pages of magazines. Print has evolved from paper to the Internet where DIY hardware projects are for sale on Mouser.com. Mouser stocks the widest selection of the newest products with same day shipping. What are you waiting for?

For more information visit: www.mouser.com

Many of the developments mentioned here and more will be on display at Mouser’s booth (Hall 4A- Stand 302) at the upcoming Embedded World show in Nuremburg, Germany, 26-28 February. Visitors to the booth will be able to discuss their requirements with our expert team and are guaranteed that we’ll have the latest available technology on display.

So-Light research project gives OLED technology a boost

By Christoph Hammerschmidt

ELEVEN GERMAN OLED companies and research institutions successfully completed the So-Light project which addressed the complete value chain, from primary materials to lighting applications. Within the project several promising innovations have been created which now will be introduced to markets.

In the project, results were achieved in a large number of technology segments, including materials, processes and panel technologies. In the field of materials, Novaled and Sensient jointly developed a new p-doped hole transport system with potential for lower absorption and lower cost scalability than previous materials. The jointly developed materials will be commercialized by Novaled. In addition, Novaled made significant progress towards a fully air-stable n-doped electron transport layer. After more R&D work it is expected that this will lead to a commercial offering. Sensient developed new host materials for OLED emitter layers which gave rise to efficiency enhancements in a reference OLED. The University of Muenster, together with Sensient, synthesized new platinum(II)-complexes. Used as triplet emitters, they enabled outstanding high quantum efficiencies for Pt(II) complexes of up to 75% (for green) and high current efficiencies of up to 16cd/A (green-yellow colour). In the processes arena, semiconductor equipment manufacturer Aixtron and the Fraunhofer research insti-

tute for organic electronic materials, COMEDD, jointly optimized the OVPD (Organic Vapour Phase deposition) process on a Gen2 substrate size. In addition, Aixtron demonstrated a new high deposition rate process based on their novel STExS source concept. Evaporation rates of above 40 Angstrom/second were achieved for the p-HTL system with significantly reduced thermal exposure of the materials involved. This will allow much faster processing of sensitive organic materials compared to the current conventional process technology. Ledon OLED Lighting developed an efficient and robust electrical contacting technology which also enabled better system efficiency and homogeneity. In addition the use of a special rear surface heat distribution unit gave rise to better OLED emission uniformity without materially altering the level profile of an OLED panel. Siteco manufactured a suspension luminaire containing OLEDs, point source LEDs and an exterior luminaire for building façade integration And BMG MIS developed a thin OLED backlight for LCD-signage application. These elements form the basis for a modular construction of ultra thin large area LCD- signage for the transportation business. The So-Light project has been supported and by the German federal research ministry with €14,7 million.

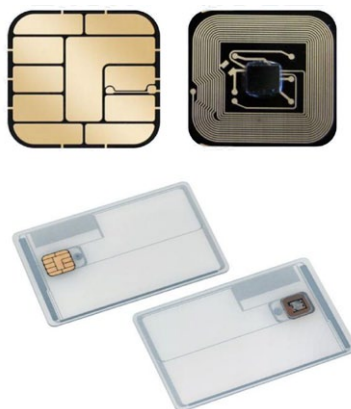


« Coil on Module » chip package could help ramp-up adoption of dual interface smart cards

By Julien Happich

INFINEON HAS INTRODUCED a 'Coil on Module' chip package that the company says will simplify the assembly and manufacture of dual interface smart cards, for a faster adoption of contactless payment applications. Dual Interface cards, which are used for both contact-based and contactless applications, are a fast growing segment of the global payments industry. According to market research firm IMS, the share of dual interface cards used in the global payment chip card market could rise from 18.9% in 2012 to 70.5% by 2017 when over 3.5 billion payment and banking cards could be shipping.

Currently, manufacturers of dual interface smart cards have to connect the chip module to the card's embedded antenna via soldered connections or conductive paste. "Special equipment and rather costly investments are required to make that extra mechanical-electrical connection, and there is a capacity shortage to fulfil the growing market for dual interface cards" explained Thomas Rosteck, Head of the Business Line Secure Mobile & Transaction of Infineon's division Chip Card & Se-



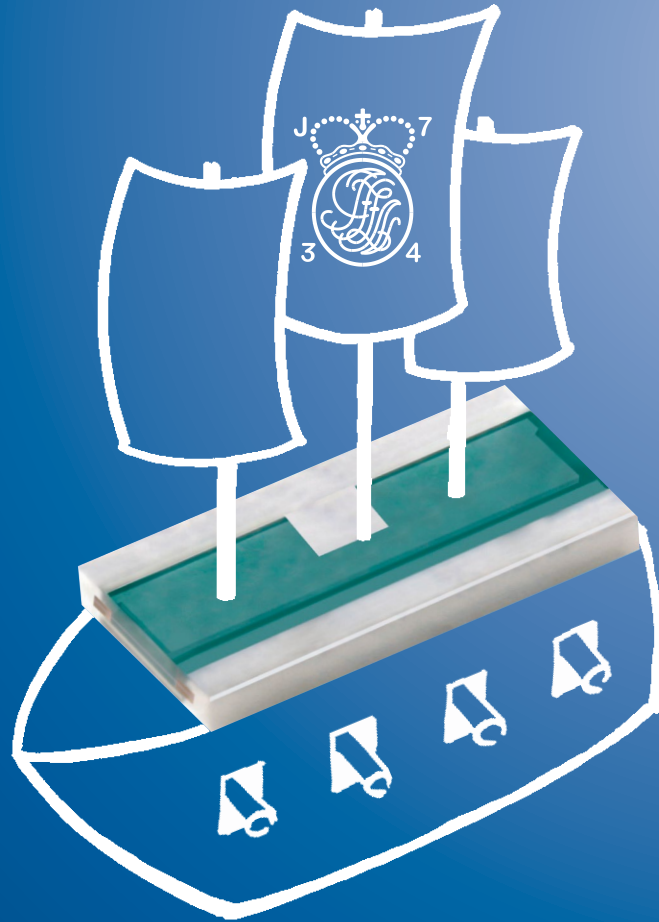
curity. "Our 'Coil on Module' solution enables card manufacturers to ramp up volumes with a simplified production process, better yield and overall lower manufacturing costs than with conventional dual interface modules" he added.

The new 'Coil on Module' package combines a security chip and an antenna that makes a radio frequency connection to the antenna embedded on the plastic payment card, through inductive coupling. Thanks to the RF link, the 'Coil on Module' technology removes the need for a mechanical-electrical connection and makes the cards inherently more robust. It

also simplifies card design and manufacturing, making it more efficient and up to five times faster than with conventional technologies, according to Infineon.

The RF coupling technology used between the 'Coil on Module' package and the embedded antenna on the card is not new per se, admitted Rosteck. It took several years for Infineon to develop the 'Coil on Module' package, the technology shares some patents from French start up Smart Packaging Solutions (SPS) - www.s-p-s.com.

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Flash Forward at the leading edge?

By Peter Clarke

SANDISK CORP. (Milpitas, Calif.), a leading supplier of data storage products, has announced it intends to begin the transition of its flash products to 1Y-nm generation semiconductors in the third quarter of 2013.

The company is already producing high volumes of 19-nm based products, more than 50 percent of its output in 4Q12, although 24-nm flash memory will have a “tail” that will last throughout 2013, the company said in a recent conference call to discuss its 4Q12 financial results.

In fact SanDisk’s announcement means that Flash Forward Ltd., a manufacturing joint venture between Toshiba and SanDisk with a relatively new Fab 5 300-mm wafer fab at Toshiba’s Yokkaichi campus in Mie prefecture, Japan, will be making close the most miniaturized commercial integrated circuits in the history of the semiconductor industry. That is unless one of the few rivals, IM Flash Technologies, Samsung or SK Hynix can get there first.

The SanDisk roadmap has the 1Y-nm process lowering the cost of 128-Gbit memory ICs in 2013 and a 1Z-nm process taking monolithic memory to 256-Gbits in 2014. But judging who is most miniaturized all depends on how you define the 1Y-nm generation.

Over the last few years flash memory producers have started to become increasingly coy about declaring the minimum feature size of their processes. It started when one of the companies, I forget which, started talking of 30-nm class and 20-nm

class manufacturing processes. By this the company meant a process with a minimum geometry between 30-nm and 39-nm and between 20-nm and 29-nm, respectively.

The other manufacturers quickly followed suit.

The psychology seems to be that if a company went public with the geometry detail before they got into volume manufacturing there would be concerns that a rival would somehow trump them and steal business. Of course once a product is out on the market it is possible for reverse engineering consultancies to cross-section chips and make independent assessments of the minimum geometry.

This is way of labeling chip generations is slightly different to the logic business where for each node a number is given but the nomenclature is becoming increasingly arbitrary. We have the prospect of 16-nm and 14-nm FinFET nodes coming in 2013 or 2014 that will use 20-nm back-end processes and are effectively 20-nm processes.

What we now know is that for Flash Forward, Toshiba and SanDisk, the 2X-nm node is a 24-nm node, while the 1X-nm node is 19-nm node. This would seem to put 1Y-nm at somewhere around 15-nm or 14-nm. That would give some room for the 1Z-nm generation to come in at 11- or 10-nm, which is now being touted as the last possible generation of NAND flash. We will see.

Nano-positioning system relies on magnetic levitation, achieves 10nm resolution

By Julien Happich

IN COOPERATION WITH the IMMS (Institut für Mikroelektronik- und Mechatronik-Systeme) and the Department of Mechatronics of Ilmenau University of Technology, Physik Instrumente (PI) has designed a novel nano-positioning system based on magnetic levitation. The platform levitates on a magnetic field that is generated by six coils and is actively monitored via a 6-D sensor. The magnetic field functions as a drive and actively guides the platform. The drive and the compact high-resolution measurement system with six degrees of freedom were developed so that the platform remains passive, in other words no cable connections are necessary. A two-dimensional, optically incremental measurement system records the position with capacitive sensors and serves to control the drive in all axes. In this way, objects can be moved linearly or rotationally on a plane with a previously unattained guiding accuracy.

“Currently, the PIMag 6D’ which is already quite an advanced development study can position with a resolution of 10 nm”



explains Dr. Rainer Gloess, Head of Advanced Mechatronics at PI.

Such a nano-positioning system could replace air-bearing solutions and magnetic linear motors typically found in inspection and manufacturing systems, in the semiconductor industry.

“If the system moves on a circular path with a diameter of 100 nm, for example, the maximum deviation from the ideal path is only a few nanometers”,

added Gloess. The current prototype has a motion range of 100x100x0.15mm³ and supports trajectory motions at an acceleration of up to 2m/s² and a velocity of up to 100 mm/s, with nanometer precision.

The digital motion controller, based on a modular system from PI, can process different geometry files as well as coordinate transformations and offers an optimum basis for a successful new product line. Physik Instrumente’s new nano-positioning system: the passive rod levitates on a magnetic field, which actively guides it.

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Taking a new direction with analog

By Paul Buckley

WITH THE INTRODUCTION of the MCP19111 single chip solution, Microchip is claiming the world's first digitally enhanced power analog controller. The company has integrated an analog-based PWM controller with a fully functional Flash-based microcontroller to offer design engineers the flexibility of a digital solution with the speed, performance and resolution of an analog-based controller.

The launch of the mixed-signal device marks a key development for Microchip and according to Stephen Stella, Microchip's Product Marketing Manager Analog & Interface Products, it indicates a new direction for Microchip's Analog division.

"Although Microchip is best known for microcontrollers we do have a significant analog group," explained Stella. "Microchip is known for being profitable. After all we have achieved 88 quarters of consecutive profitability. The Analog division has helped that profitability and started around the 2000/2001 period when we acquired a company by the name of Telecom Semiconductor that gave us a fundamental start to our analog portfolio. The Analog business has grown steadily since 2001 but in the last two years we have seen a significant growth in analog revenues".

There are currently 28 product lines within Microchip's analog portfolio which cover a wide array of analog-type peripheral devices that surround the microcontroller. The company now has more than 830 products in the Analog business portfolio and the number is growing rapidly.

"The key ones in our linear group include a very broad array of operational amplifiers that are used in sensor-type applications," explained Stella. "However, power management is becoming a key investment area for Microchip."

"Seeing this growth Microchip's leadership team has continued to invest in analog technology and analog design, the outcome of which are new products like the digitally enhanced power analog controller and new processes that we are developing".

Stella continued: "Microchip's standard analog strategy has been historically supporting the microcontrollers business. As the Microchip microcontrollers are designed in products, there are a lot of components that go around them to enable the microcontroller in its application. Historically our analog strategy has been to attach ourselves to the microcontroller be it as amplifiers or ADCs or LED drivers or power MOSFET drivers. What the analog development team does is to enable the microcontroller to do what it needs to do in a particular application. We are now expanding the scope of that strategy not just to Microchip microcontroller type applications but also to stand-alone full analog applications".

"We recognize that there is an integration path on the microcontroller side where a lot of the simplistic analog capabilities are being pulled into the microcontroller. Even though the requirements intensify it still makes sense to do things outside the microcontroller. If you look at an A-to-D conversion then it is clear that for some 24-bit super high-

speed A-to-D converter the process technology needed to handle that does not necessarily match up to the process technology needed to support an 8-bit micro. Most of Microchip's 8-bit business is in simple embedded controllers".

"At least 90 percent of our products are for one-stop shopping," suggested Stella.

"Microchip has not historically been an innovation leader in the analog space. In the past, the developments have been really to supplement the microcontrollers that we have. But now we are starting to do new and interesting things that no one else is doing. As we take those enabling technologies we are starting to focus more on six core application areas".

These core application areas are power and flow metering (which relates to power monitoring and energy metering); smoke and carbon monoxide detectors; PC/laptops/servers and gaming; consumer type devices; temperature measurement; and power supplies.

"Each one of these applications is a power management sub-application," explained Stella. "All of them use and need power management type devices and all of them have unique requirements. We have recognized this and have started to put applications support behind them to leverage all of the strengths and capabilities and products within Microchip to develop valuable solutions for our customers."

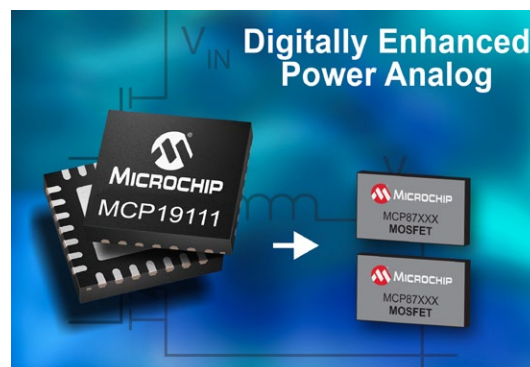
"There is an application need for Microchip to support higher voltage technologies," advised Stella. "We want to start building that into our portfolio. That has opened us up to some higher power applications so we went to driving higher current and that made us look at how we should support higher current applications. And as you extend into even higher power applications then efficiency becomes more and more of a key factor. So we need to look at how we can make solutions that enable our customers to achieve higher efficiency in their target applications".

"The high level application areas being addressed by the new digitally enhanced power analog controller will focus on computing, consumer and communication," explained Stella.

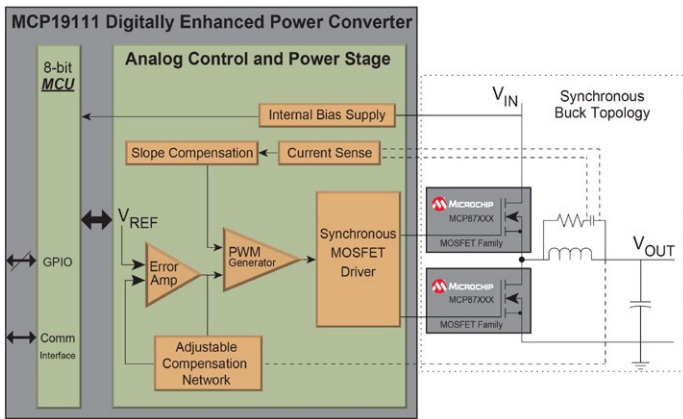
"These are DC-to-DC point-of-load type of applications. Microchip has its dsPIC device on the digital serial controller side which handles power levels



Stephen Stella, Microchip's Product Marketing Manager Analog & Interface Products takes Microchip's Analog division into a new direction.



The MCP19111 digitally enhanced power analog controller.



The MCP19111's block diagram.

of 300 W and above whereas our analog portfolio is handling 50 W and below. But the new digitally enhanced power analog controller focuses on an intermediate area which is some place between 50 W and 150 W.”

“Over the past two or three years we have seen an introduction of a hybrid control-type topology or mixed-signal-type topology where there is a component of analog and there is a component of digital. There are different ways of developing these kinds of solutions. We are seeing on the microcontroller side continued integration of analog-type peripherals whereas on the digital side it is a little bit more difficult to integrate technologies because of process differences. What we saw as an opportunity was a digitally enhanced power analog controller”.

“We have retained the performance of the analog control without introducing the need for a high-speed, high-performance microcontroller. That typically means a very small lithography type process which is less expensive. The same thing applies with the analog-to-digital conversion element.

The solution needs to be of high precision for load regulation accuracy and it also needs to be of high speed for the same bandwidth concerns that you have if you try to convert it into a digital domain. So you eliminate cost and you eliminate complexity. And when you eliminate that complexity it also enables some additional integration on the analog side”.

Stella continued: “Yet it still offers digital flexibility because with the small microcontroller you can actively optimize the analog. That allows you to offer ‘configurable analog’ solutions which is something new because you don’t normally hear the words ‘configurable’ and ‘analog’ in the same sentence”.

“Essentially we have the 8-bit MCU while also having the analog controller with an integrated MOSFET driver and an integrated LDO. The device offers the fully programmable MCU core which enables the custom IP integration that customers tell us they are looking for and allows them to do custom firmware development “.

“This device is more than just a controller it can turn into a system architecture power management device because it can now be used to control the turn on of various voltage regulators within a system. With load complexity increasing and with advanced devices like FPGAs requiring certain timing sequences and voltage rail performance you can now have a central device that could help you sequence your power management needs”.

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3D noise cancellation makes voice control significantly more reliable

By Lior Blanka

VOICE QUALITY IS becoming a hot issue due to the recent rise of voice control interfaces for tablets, computers, Smart TVs and other consumer electronic devices. Without intelligible speech, automatic voice recognition can't function properly nor be relied upon as a form of device control. This problem is compounded by noisy environments that can severely degrade the quality of speech to the point where voice control is totally inoperable.

Traditional noise cancellation suffers from trade-offs between the degree of noise reduction and voice quality: the higher the noise reduction levels, the greater the potential for voice distortion. Attempting to minimise the trade-offs, engineers have developed Noise reduction algorithms to reduce the amount of noise which perform well mainly in stationary noise and poor performance in non-stationary noise such as street noise and similar other noises.

Noise cancellation technique took a leap forward with the introduction of a second microphone in smart phones, enabling both microphones to operate in similar manner to the human auditory system. However, this capability does not provide sufficient noise cancellation to eliminate all background noise for voice calls or voice control, while driving or riding on public transportation, or even at home when, for instance, music is turned up loud.

Adding a sensor for advanced noise cancellation

Advanced noise cancellation technology uses an additional sensor in addition to the standard two audio microphones, and then applies a 3D-Vocal algorithm to perform multiple voice processing tasks including echo and background noise cancellation, loudness equalisation and general voice enhancement. Removing background noise significantly improves the accuracy rate of ASR, (Automatic Speech Recognition) and voice-call applications for smart phones, tablets and other mobile devices.

An example of how the advanced noise cancellation affects

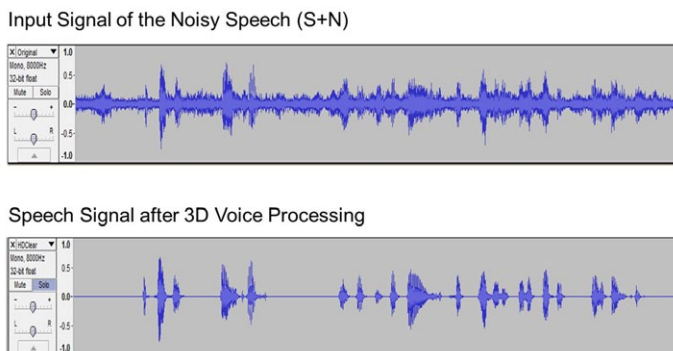


Fig. 1: Typical 3D voice processing results on speech and ambient noise.

Lior Blanka is Corporate Vice President and Chief Technology Officer of the DSP Group - www.dspg.com

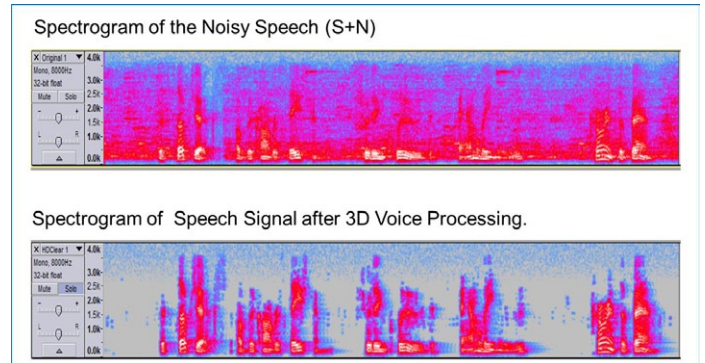


Fig. 2: Spectrogram of 3D processing on speech and ambient noise.

the noisy speech is shown in figure 1. The upper waveform illustrates the noisy speech that is the superposition of speech and ambient noise (S+N), while the lower waveform shows the clean speech signal after 3D voice processing.

Figure 2 shows a spectrogram, where the upper graph presents the spectrogram of the noisy speech S+N, the lower spectrogram shows the resulting speech signal after 3D voice processing. Using the expanded set of data provided by the sensor and the two microphones, the 3D-Vocal algorithm extracts features that characterise the speech source and distinguishes between the sound components that belong to required speech vs. ambient noise. The block diagram in figure 3 shows the audio path for the advanced noise cancellation technique.

3D voice processing diagram components

The 3D-Vocal (Spectro-Temporal Analysis) consists in receiving all the signals from the microphone array and from the VSensor, and performing special spectro-temporal processing on the combined information. Some correlated patterns in the 3D-Vocal data are associated with ambient noise, while others are identified as the user's voice. The 3D-Vocal spectro-temporal process separates the user's voice from the predicted ambient noise and produces some reference information for the voice/noise Feature Extraction block.

With Feature Extraction, voice/noise data is fed to the other blocks. The extracted features contain spectro-temporal, real-time information about the user's speech and ambient noise. This information can be used to filter out ambient noise from the user's speech, enhance echo cancellation performance, and more. Ambient Noise Cancellation cancels various types of stationary and non-stationary, coherent and non-coherent ambient

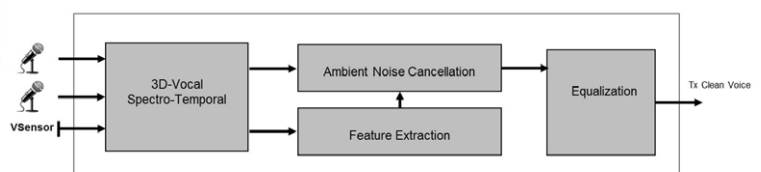


Fig. 3: Block diagram for 3D voice processing.

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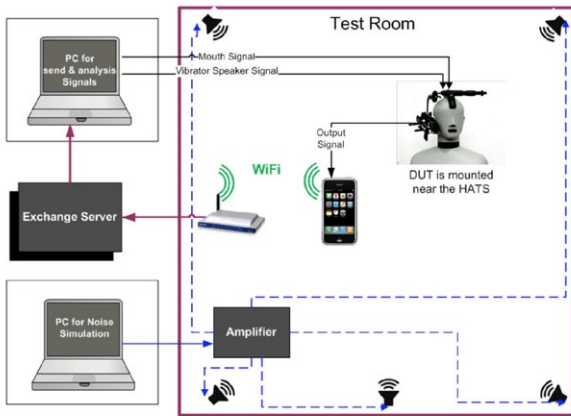


Fig. 4: Word error rate test set up.

noise. The ambient noise cancellation algorithm uses feature extraction information and the output of the 3D-Vocal block.

Equalisation is performed to equalise the spectral distribution of the received signal to match the requirements of the ASR process or the voice call requirements.

Minimising word error rate for speech recognition

To evaluate how the improved voice quality impacts the performance of a virtual assistant, a test was conducted measuring the Word Error Rate (WER) which calculates the number of error words between the spoken word sequence and the recognised one, using the formula:

$$WER = \frac{S+D+I}{N}$$

Where

S is the number of substitutions

D is the number of deletions

I is the number of insertions

N is the number of words in the reference ($N=S+D+C$) with C being the number of correct words.

A voice script was dictated using a commercial virtual assistant system on a mobile phone with 3D voice processing and with 2D voice processing. The script was dictated in different background noise type, such as a cafe, a pub, a car and a train and the WER was calculated with 3D voice processing and with 2D voice processing. The test benchmark was performed using the set up described in figure 4, all the tests being performed in an acoustic chamber which included a Head and Torso Simulator (HATS). The mobile handset under test was positioned attached to the head of the mannequin.

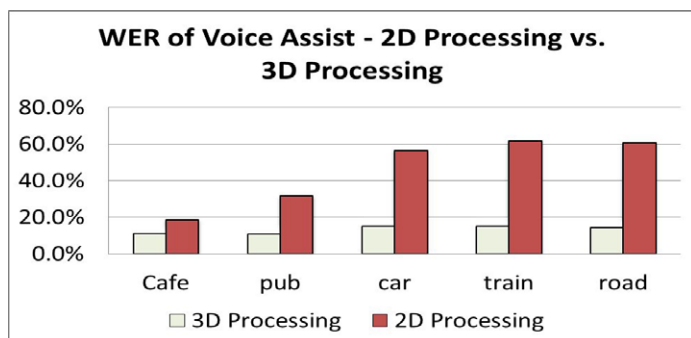


Fig. 5: Increased virtual assist reliability with 3D voice processing.

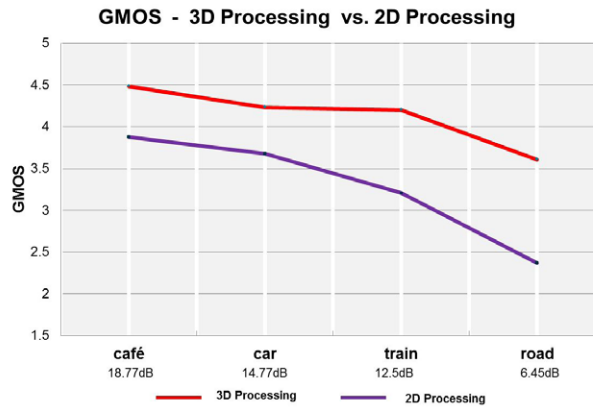


Fig. 6: GMOS as a function of noise type for 3D voice processing and standard 2D voice processing.

Background noises per ETSI EG 202 396-1 was injected to four loudspeakers and a subwoofer by a PC which triggered by the Master PC. The “dictated clean speech” is played by the mouth of HATS that is fed from the Master PC via the analogue front

end (Head Acoustics’ Measurement Front End, MFE VI.I). The speech captured by the mobile phone is converted to text email by the virtual assistant, and the WER was then calculated by analysing the received text mail.

The result of the test is presented in figure 5. With 3D voice processing the WER is in the range of 10 to 15% for all the noise types, while with 2D voice processing, the WER ranged from 18 to 60% and depended on the noise type, which means that ASR with 2D voice processing in a noisy environment is not consistent. In some noise types it will work fine and in other noise types the performance can be very poor. However, as shown on figure 5, with 3D voice processing, ASR degradation remains minimal and consistent for all noise types, making the virtual assistant significant more reliable.

Improving the quality of voice communication

By incorporating the advanced noise cancellation capabilities into smart phones for voice communication, the voice quality can be significantly improved from “poor” to “very good”. The audio quality of 3D voice processing was compared with standard 2D noise cancellation techniques using the ETSI EG 202 396-1 standard, which defines a method to test the quality of noise reduction algorithms objectively. The scale for general quality (GMOS) is shown in Table 1. Voice quality was compared according to the MOS scores using a standard phone with built-in 2D voice processing in different types of noisy environments. Figure 6 shows that the score of the 3D voice processing is significantly higher than the standard 2D voice processing.

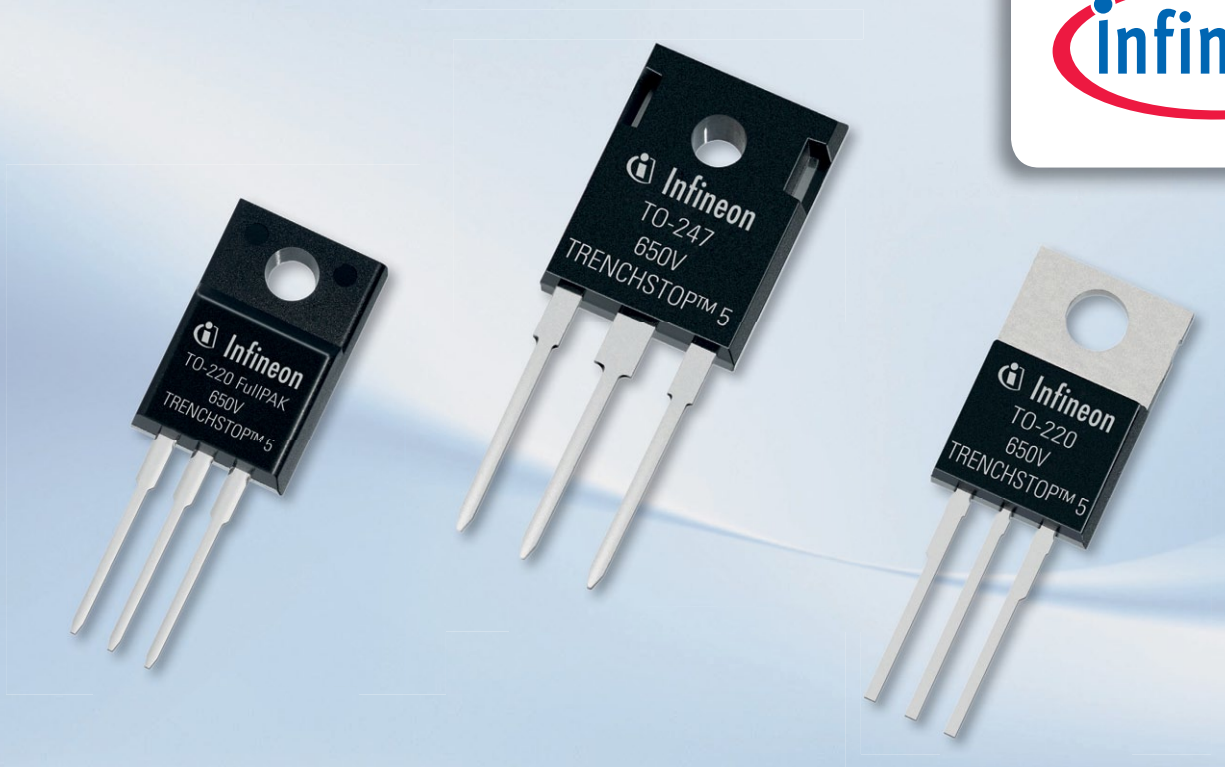
Value added 3D voice processing

For safety and convenience reasons, hands free operation will often be the first choice for consumers. And yet voice control is just beginning to see its true potential. Test results indicate that 3D voice processing can significantly improve the reliability and usability of voice control enabling it to become a valuable differentiator.

In addition to better voice control for smart phones, tablets, and a wide range of consumer electronic devices, 3D voice processing supports the injection of background music or sounds during on-going conversations. This could provide telecom service providers with new services that could be available at a premium, generating more revenue.

SPEECH QUALITY	Rating
Excellent	5
Good	4
Fair	3
Poor	2
Bad	1

Table 1: General MOS scores (GMOS).



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Designing low-power video image stabilisation IP for FPGAs

By Dr S. Parker and W. Cranwell

IMAGE STABILISATION IS an important capability for many electro-optic sensors, where an operator or user is required to view the output imagery. The technique can therefore enhance many practical viewing systems, spanning a very broad range of applications including those found in defence and security sectors. Stabilisation provides a means for reducing both image blur and unwanted frame-to-frame image shifts and rotations, thereby aiding image interpretation and reducing the operator's workload. For those systems that require the operator to locate or classify features within the video stream (typically recognition and identification), then a stabilised image stream will help improve the accuracy of these tasks.

There are a number of techniques for stabilising an image which are either based on mechanical correction or image processing. Mechanical stabilisation techniques include those that gyroscopically stabilise the whole camera system or use elements within the camera to effectively move the lens or detector array. Mechanical stabilisation techniques are well established, although they can have a limited rate of response. Furthermore, they tend to be more expensive, consume more power and are physically larger and heavier. Mechanical stabilisation techniques used within the camera housing are generally less expensive and are physically more compact. However, they can have performance limitations such as an inability to correct for roll, and may operate over a restricted range of unwanted camera movements. In addition, such integrated camera techniques are less well established for infrared cameras and those cameras that use interchangeable lenses. Finally, it should be noted that mechanical stabilisation corrects for movement associated with the camera, but does not correct for other effects such as atmospheric scintillation.

Digital video stabilisation techniques provide image correction by using information from within the video-stream and this includes movements of the camera, any atmospheric effects,

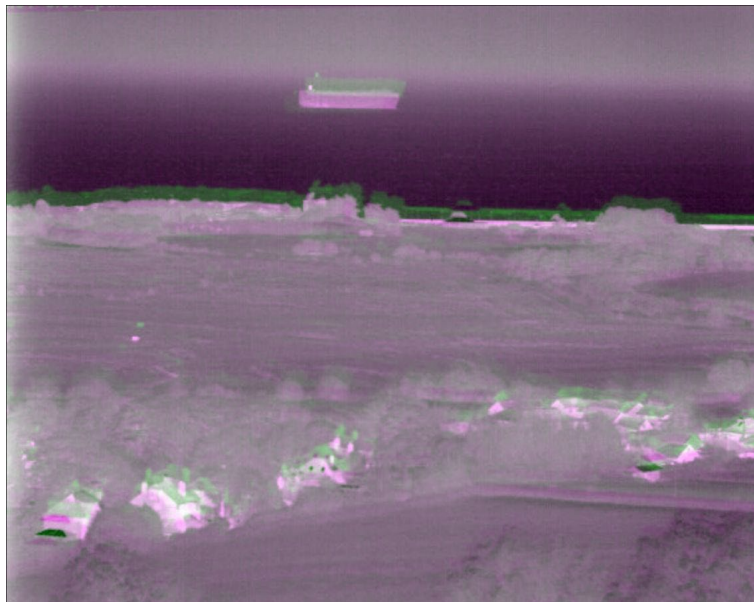


Fig. 1: Unstabilised image set. The 5 frames have been false-coloured and superimposed to illustrate the movement effect.

and movement within the scene itself. The approach offers a potentially significant performance gain with minimal impact on power, weight, and size. However, to realise these benefits, the stabilisation algorithm complexity can be high, which translates into a high computational load. Although electronic stabilisation can be achieved using a low-cost CPU architecture, the limited processing bandwidth restricts the maximum input image size and frame rate. Consequently, the capability of the stabilisation algorithms has to be compromised to facilitate real-time operation. GPU architectures can be used to reduce the limitations

associated with CPU-only devices and provide higher processing bandwidths that enable more complex processing. However, GPU implementations consume more power and often still need an additional system host for designs based on commercial-off-the-shelf products.

The approach taken by RFEL has been to specify a high-performance stabilisation system that can readily support high input resolutions and frame rates, while maintaining low latency and power consumption. Also, the solution was required to be compatible with cameras that operate over different spectral bands, with support of multiple camera interfaces.

Physically, a flexible and compact hardware implementation was required that supports both stand-alone and networked applications. Furthermore, the stabilisation solution should allow rapid integration into third-party hardware, including retro-fitting into in-service equipment.

To meet these challenging requirements, RFEL elected to base the implementation on the latest FPGA architectures which have embedded ARM processors. Compared with a GPU implementation, the primary drawback was the required engineering development time which is significantly higher when compared with a CPU / GPU software module implementation. Fortunately, RFEL has been developing advanced signal and video processing modules for many years, which allowed substantial re-use of pre-existing functions and development tools.

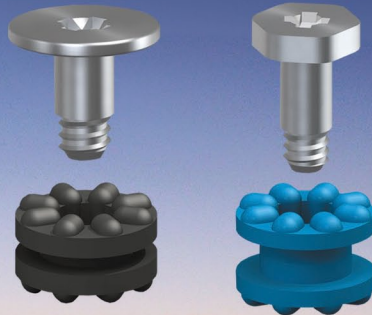
Initially, functional requirements were captured by liaising with major customers in the military and security markets.

The system was then designed and developed using RFEL's proven methodology of floating and fixed-point modelling in Matlab that allows efficient performance testing, rapid debugging and substantially de-risks all aspects of system implementation.

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Wayne Cranwell is Technical Sales Engineer and Project Manager at RF Engines Ltd – he can be reached at Wayne.cranwell@rfel.com

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A fundamental challenge in the development of any video processing product is the complexity and diversity of the imagery that must be processed by the product for the large range of applications. Experience has shown that the development of a video processing function, with testing confined to only a limited data set, can introduce significant programme risk as discovery of 'corner case problems' late in the development may necessitate substantial rework. Consequently, RFEL performed a series of trials using various cameras and platforms, with imagery gathered at different times of the day and under various weather conditions. The data gathered was sufficiently diverse to give confidence that the stabilisation design would be fit for purpose for land, maritime and airborne applications.

Several contrasting approaches can be used for electronic image stabilisation. The first, and most popular, is the use of prominent image features to generate frame-to-frame flow vectors. Typically, this approach involves feature detection and tracking of these features between frames. If the frame-to-frame movement is assumed to be low and high detection thresholds are used then the implementation can be relatively simple. However, performance and robustness when operating with diverse imagery can be poor.

An alternative approach, adopted by RFEL, is to process image frames on a tile basis in the spatial frequency domain. Such an approach determines the stabilisation corrections through the analysis of much more scene information and can operate effectively even when the scene contains no high-contrast prominent features. Consequently, the spatial frequency approach lends itself to a more robust and accurate stabilisation solution, albeit at the price of a significantly higher processing complexity.

In terms of the derived requirements, the RFEL stabilisation function was specified to deliver a stable image under the most demanding of applications covering: driving aids for military vehicles, diverse airborne platforms, targeting systems and remote border security cameras. Furthermore, the algorithm design was required to stabilise images subjected to two-dimensional translation and rotation from both static and moving platforms. It is envisaged that the stabilisation function will be used for supporting many different physical equipment installations. As such, the centre of rotation could be within the camera or external to it and the stabilisation algorithm must be able to cope with such installations.

The stabilisation function was required to provide real-time correction at frame-rates of up to 150Hz for various imaging devices and for resolutions of up to 1080p including both daylight and infrared cameras. For example, a 1080p colour camera operating at 8-bits and with a frame-rate of 60Hz, necessitates operation with an input data rate of about 1 Gbits/s.

An FPGA-based hardware implementation provides the computational resources needed to process several gigabit/s

input data rates with the selected spatial frequency stabilisation method. However, even with the inherent processing power of an FPGA, the implementation has to be carefully tailored to satisfy the stringent latency and power consumption constraints. Given that the stabilisation function is likely to be only one component of a larger processing suite, it was also necessary to minimise the number of gates and external memory accesses used.

The level of stabilisation accuracy achieved under a very diverse and demanding range of evaluation test data was typically less than ± 1 pixels, even when subjected to random frame-to-frame displacements of up to ± 25 pixels in x and y directions and with a frame-to-frame rotational variation of up to $\pm 5^\circ$.

The performance of the stabilisation function is illustrated with figures 1 and 2, using a small number of frames from a daylight camera.

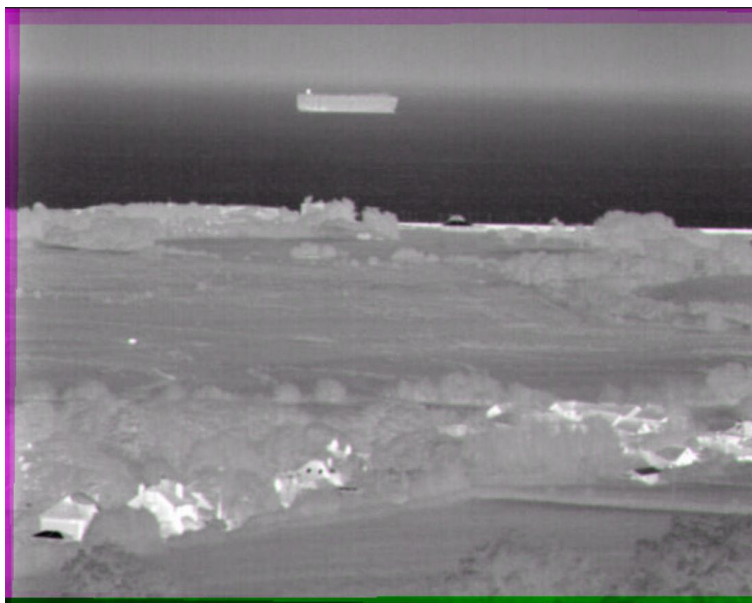


Fig. 2: Stabilised image set. The rotation correction can be readily gauged from the edges of the image frame.

The performance of the stabilisation design is shown using five consecutive frames from a sequence, when subjected to a random frame-to-frame rotation as large as $\pm 1^\circ$ around the centre of the image.

The design has proven to be extremely flexible and can be used for both static and moving camera platforms. Although this capability can be delivered through an FPGA-only implementation, further capability and performance can be achieved through additional software functions hosted on the ARM multicore processors embedded in the latest FPGAs.

The stabilisation design was originally implemented on

a development platform for Xilinx's new Zynq-7000 All Programmable SoC, which hosts an ARM Cortex-A9 MPCore dual core processor. This development board allowed early revisions of the design to be matured based upon target device resource and processing constraints. The processor was accelerated by exploiting existing RFEL's IP Core components that reside in the fabric of the FPGA and have been optimised and tested over the last 10 years. A specific hardware design was also undertaken that provides the stabilisation IP Core, together with other video processing functions, in a fully integrated custom hardware system-on-module. This module can interface with many different standards such as Analogue, CameraLink and GigE based protocols such as GigEvision.

RFEL's video image stabilisation processing capability is now available as an IP Core, optimised for FPGA. The fully integrated hardware system-on-module that incorporates the stabilisation function will be available in Q2/2013 and may be ruggedised to military standards. This stabilisation system offers exemplary performance even when the camera is subjected to extreme unwanted shifts and rotations. When this capability is coupled with a low power and low latency implementation, the design becomes highly suited to military and security applications, as well as more demanding commercial applications. In addition, the IP Core can be readily integrated with existing processor hardware with negligible impact on size and weight.



Testing HDMI and MHL successfully

By Harald Gsoedl

TODAY'S SET-TOP BOXES, tablet PCs and smartphones are equipped with analog or digital video interfaces such as the high-definition multimedia interface (HDMI) and the mobile high-definition link (MHL). Manufacturers test these interfaces at different stages in the value chain to verify their functionality and compliance with standards and thus ensure that they operate flawlessly when they reach consumers. Besides pure interoperability tests, manufacturers are also conducting an increasing number of application tests to see how equipment performs under realistic conditions.

The high-definition multimedia interface

When HDMI technology was first introduced in 2002, it triggered a paradigm shift within the consumer electronics industry. For the first time, equipment manufacturers and content providers alike embraced a digital video and audio interface standard. Since 2002, more than a billion electronic devices equipped with HDMI have been manufactured. Prior to the introduction of HDMI, consumer electronics equipment typically used analog interfaces to transmit video content, in spite of the known shortcomings compared to digital interfaces.

The main reason behind the reluctance among content providers such as Hollywood studios to make the transition from analog to digital was that digital versatile discs (DVDs) or digital video broadcasting (DVB) could potentially allow lossless duplication of content by pirates, directly over external ports.

HDMI succeeded in eliminating these concerns. This is because HDMI uses a special encryption mechanism – high-bandwidth digital content protection (HDCP) – to secure content against duplication. If this is enabled on the source device (a Blu-ray™ player, for instance), the sink is checked to determine whether it supports HDCP. If it does, the source and sink exchange an encryption key that is used to decrypt the transmitted data.

HDMI's technical design also ensures that video and audio content is transmitted in high quality, with little interference. The data is transferred between devices via three high-speed channels known as transition minimized differential signaling (TMDS) lines. In the most recent version of the interface, these channels are specified to support a bandwidth of up to 3.4 Gbit/s each. The interface also incorporates control lines, as shown in figure 1.

Going forward, the focus will be on introducing ultra-definition (UD), which offers resolutions far higher than the 1920 x 1080 pixels currently supported by Full HD. This will take resolutions like 4K x 2K, already widespread in movie theaters and studios for some time now, into people's living rooms. The demand is there: displays are getting bigger all the time, the first consumer video cameras capable of this kind of resolution are already available, and people are using TVs more and more as an alternative to personal computers.

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Mobile high-definition link

Mobile high-definition link is a new standard closely related to HDMI. This new interface technology is most common in smartphones. It allows content such as Internet-streamed media, movies and user-created video to be output to TV screens in HD resolution.

MHL runs on the micro-USB port now included in many mobile devices. MHL consortium founders Nokia, Samsung, Silicon Image, Sony and Toshiba point to the new technology's following benefits for mobile applications:

- The micro-USB port can be used to transmit uncompressed HD video and audio.
- Mobile devices can charge while playing media.
- Eliminating the need for a separate audio/video port – combined with micro-USB's small size – enables manufacturers to produce even smaller smartphones.

The USB port is used to exchange data with a personal computer as usual. However, if the built-in MHL transmitter chip detects that it is connected to an MHL enabled sink or MHL to HDMI converter, it switches automatically to MHL transmission mode. In this case, the MHL transmitter sends the audiovisual data across the micro-USB connection.

Like HDMI, MHL has an additional pin for transmitting control signals. This is for the MHL control bus (CBUS), which performs various tasks: It detects whether an MHL enabled sink or source is connected, and it transmits data relating to the encryption of audiovisual data. The MHL voltage bus (VBUS) has a 5 volt line carrying a maximum of 0.5A, which is powered by the MHL sink.

The most recent version of MHL is V1.2. Work is currently in progress on V2.0, which will extend the standard. Future versions will add new capabilities,

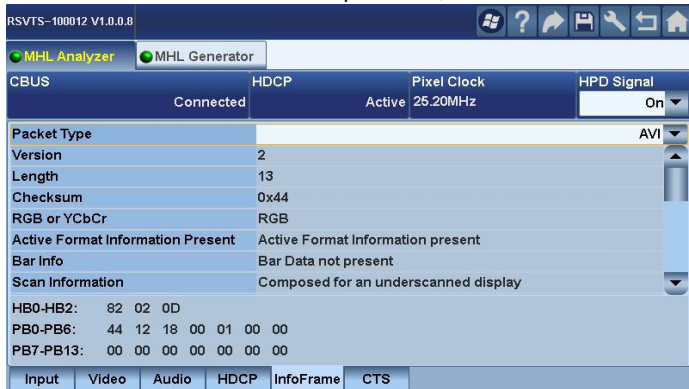


Fig. 2: Auxiliary video information (AVI) InfoFrames.

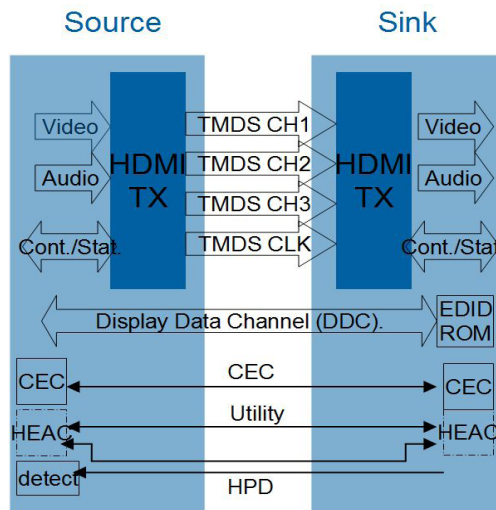


Fig. 1: Block diagram showing communications between an HDMI source (e.g. a Blu-ray player) and sink.

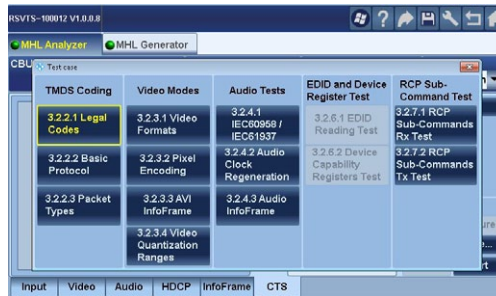


Fig. 3: Raw TMDs data is analyzed for system tests conducted in accordance with the compliance test specification (CTS).

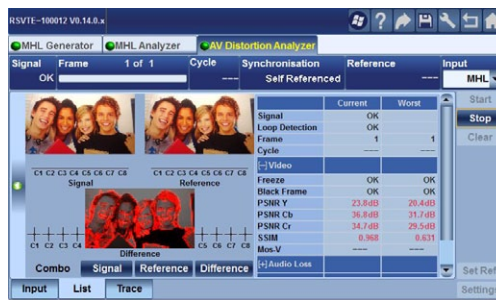


Fig. 4: Image difference analysis detects and analyzes picture errors according to the relevant metric.

such as support for 3D video formats and higher charging currents.

Interface conformity at the protocol level

Both HDMI and MHL transmit the visible video signal in TMDs frames and the audio and meta data (e.g. InfoFrames) in the blanking intervals (HSync and VSync). The purpose of the meta data is to tell a connected device about the properties of the data stream (resolution, color range, frame rate, etc.).

Consumer electronics devices' digital interfaces are tested for protocol conformance during development and certification to ensure the devices' interoperability with other equipment. During development in particular, the ability to view the following key protocol parameters in realtime is crucial:

- Video timing parameters such as pixel clock and resolution in line with CEA-861.
- Audio clock regeneration (N/CTS) and audio sample packets
- High-bandwidth digital content protection (HDCP) status and the keys used.
- Auxiliary video information (AVI) InfoFrame, audio InfoFrame, source product description (SPD) and MPEG InfoFrame.

Figure 2 is an example showing how the new Rohde & Schwarz video tester family uses MHL protocol analysis to display TMDs data. The screen shows an analysis of AVI InfoFrame data. A typical test scenario in which this capability is used is when troubleshooting an MHL enabled device that fails to switch to an expected state.

A special application is conformance testing in line with the standard's compliance test specification (CTS) as a final interoperability test. Before a device fitted with an HDMI or MHL port is introduced to the market, it must first be checked

by an authorized test center (ATC) to verify that its functionality conforms to the CTS. Tests are not just conducted at the protocol level but also on the physical layer, with separate tests for sinks (TVs), sources (set-top boxes) and cables.

The tests carried out during the certification process are both time-consuming and costly. If errors are found during certification, the entire test has to be repeated. It therefore makes sense to conduct tests using suitable T&M equipment capable of assuring devices' quality prior to the certification process.

To certify consumer electronics equipment in a lab or to conduct advance assessments, protocol tests must be carried out as described in detail in the standards under specific test IDs. The section headings in the CTS correspond to the test ID numbers. Figure 3 shows the system tests specified in MHL CTS 1.2.

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PENTEK
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Testing video applications in cellular networks

According to International Data Corporation (IDC), almost 500 million smartphones were sold worldwide in 2011. This trend will gain even greater momentum as the current rollout of Long Term Evolution (LTE), the fourth generation (4G) mobile communications, progresses. A large number of devices already support mobile multimedia reception and are equipped with video/audio interfaces that enable lossless transmission of high-definition content to TVs.

With the introduction of LTE, additional video services will become available. There are plans to introduce not just reliable high-definition video telephony, but also Internet-streamed video on demand (VOD), and TV-like enhanced multimedia broadcast multicast services (eMBMS).

During development and quality assurance, the ability of multimedia-ready mobile equipment to support these video services is assessed in application tests under deliberately degraded conditions. In the test lab, various types of interference are applied to the simulated transmission path between the base station and the mobile device that are likely to occur during real-life use. The tests simulate RF interference, apply noise to the signal, and simulate IP faults like packet loss and packet delay.

The actual application tests then detect the types of picture errors that typically result from transmission errors.

Examples of the kinds of problems that arise include blocking, freezing and even the loss of whole pictures in a se-

quence.

A typical setup for an application test like this might consist of a base station simulator such as the R&S CMW500 and an R&S VTE video tester. The base station simulator sets up a valid LTE connection and makes the audio/video data available for download through its built-in media server. An optional fading simulator also allows RF interference to be added. The smartphone decodes the data it receives and outputs the pictures on its display or plays the audio over its speakers. The audiovisual data is transmitted without loss or external impacts over the phone's HDMI or MHL port to the video analyzer, where it can be reviewed.

The transmission errors simulated cause picture errors. To record interference in reproducible form, T&M labs use image difference algorithms. These algorithms compare, in realtime, an ideal reference against the image sequence being tested. The difference between the images is then computed, both graphically and numerically. Figure 4 shows the T&M interface for image difference analysis on the R&S VTE. Support for common industry metrics such as peak signal-to-noise ratio (PSNR) and structural similarity (SSIM) means that image evaluations are reproducible and can be automated.

The PSNR and SSIM are computed for individual images. However, to assess the visibility of errors occurring in moving images, time masking effects can be considered by setting thresholds. This means that visible errors in a moving sequence can serve as a trigger.

To ensure that the AV interfaces and video processing in multimedia devices functions flawlessly, video content and protocols must be tested at every stage. Reproducible and conclusive test results are best achieved with T&M instruments that can be upgraded to support future applications.

The R&S VTC video test center, R&S VTE video tester and R&S VTS compact video tester as shown on figure 5 are capable of conducting the kinds of interoperability and application tests required during the development, quality assurance and manufacturing of multimedia devices with AV interfaces. Their modular hardware and software designs also mean they are capable of being expanded to support new interface standards as these emerge.



Fig 5: The Rohde & Schwarz video tester family for interoperability and application testing on AV interfaces.

Image signal processor addresses video monitoring applications

ON Semiconductor has released two highly integrated image signal processor ICs designed for use in applications such as vehicle reversing cameras, in-vehicle navigation systems and various consumer video monitoring security systems where small LCD screens are utilised. The LC749000PT for automotive applications and the LC749000AT for consumer products, support important end application energy savings and use advanced signal technology to improve the picture quality of digitally compressed images. The chips support installations with screen resolutions up to Wide Video Graphics Array (WVGA), and integrate an analog to digital converter which receives direct analog picture signal inputs from a camera.

ON Semiconductor
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Low power DSP IP core for always-listening voice trigger and voice recognition

Tensilica introduced the HiFi Mini DSP (digital signal processor) core, claimed to be the smallest, lowest power DSP IP core supporting always listening voice trigger and speech command modes. Optimized specifically for the smallest area and lowest power in smartphones, tablets, appliances, and automotive applications, the HiFi Mini DSP IP core enables a hands-free experience. The DSP core uses compact 40-bit encoding, which significantly improves code size. Tensilica added efficient 16-bit instructions optimized for voice and audio codecs.

The result is a post-route core that's only 0.039 mm² in 28 nm HPL. Using Sensory's Truly Handsfree voice control technology, HiFi Mini is able to achieve less than 88 uW of power for the core in 28 nm HPL.

Tensilica
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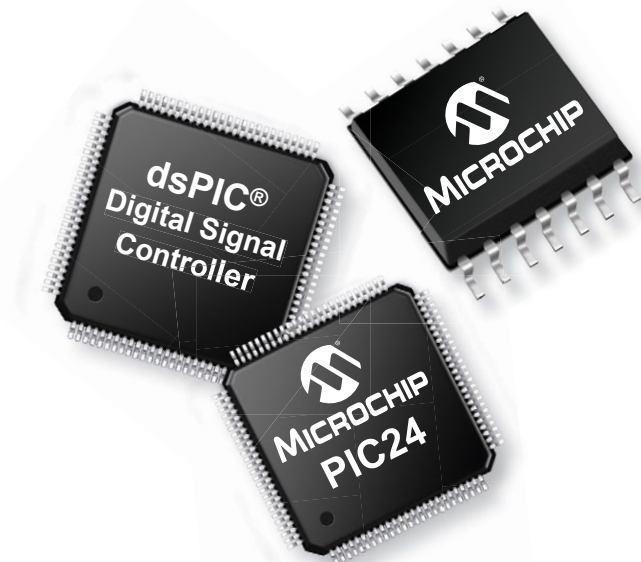
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PIC24F D Families	64–100	128–256	24–96	5 Timers 9 IC 9 OC	10-bit ADC (500 ksp/s), 16–24 ch., 3 comparators, CTMU	UART (4), SPI (3), I ² C (3), USB-OTG	Graphics Display Controller PPS, PMP, RTCC, CRC, JTAG
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dsPIC33EP MC Families	70 MIPS	28–64	32–512	4–48K	5 × 16	6–16	10 or 12	500 or 1.1M	4	UART, I ² C, SPI, CAN	6	Motor Ctrl.	Flash security, on-chip op amps, mTouch, JTAG, DMA, CRC, QEI
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Low Power Design Guide: A single source for low power consumption from the viewpoint of the MCU (Application Note AN1416)

nanoWatt XLP Technology: An Introduction to Microchip's Low-Power Devices (Application Note AN1267)

Development Tools

nanoWatt XLP 16-bit Development Board (DM240311)



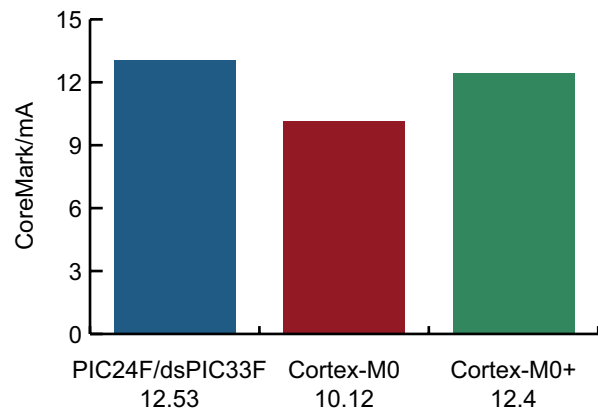
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- Industry leading PWM module ideal for motor control
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 - BLDC, PMSM, ACIM
 - Sensorless control
 - Field oriented control
 - Certified class B safety software
- Scalable motor control tools with low and high voltage options

Webinar Topics

- Sensorless Field Oriented Control for ACIM
- Sensorless Field Oriented Control for PMSM
- Sensorless BLDC Motor Control Using a Majority Function
- Brushed DC Motor Basics
- Stepper Motor Control

Software & App Notes

Motor Type	Algorithm	App Note
Stepper Motor	Full and Half-Stepping	AN1307
	Micro-Stepping	AN1307
BLDC and PMSM	Sensored	AN957
	Sensored Sinusoidal	AN1017
	Sensorless BEMF	AN901 AN992
	Sensorless Filtered BEMF with Majority Detect	AN1160
	Sensorless Dual-Shunt FOC with SMO Estimator and Field Weakening	AN1078
	Sensorless Dual-Shunt FOC with SMO and PFC	AN1208
	Sensorless Dual-Shunt FOC with PLL Estimator and Field Weakening	AN1292
	Sensorless Single-Shunt FOC with SMO Estimator and Field Weakening	AN1299
AC Induction Motor	Open Loop V/F	AN984
	Closed Loop Vector Control	AN980
	Sensorless Dual-Shunt FOC with PLL Estimator	AN1162
	Sensorless Dual-Shunt FOC with PLL Estimator and Field Weakening	AN1206
Other	PFC	AN1106
	Appliance Class B (IEC 60730)	AN1229
	Motor Control Sensor Feedback Circuits	AN894
	MOSFET Driver Selection	AN898
	Current Sensing Circuit Concepts and Fundamentals	AN1332

Featured Motor Control Products

Product	MIPS	Pins	Flash (KB)	RAM (KB)	DMA Ch.	Input Capture	Output Compare/Std. PWM	MC PWM	QEI	Internal Op Amps	ADC 10/12-bit 1.1/0.5 MSPS	UART
dsPIC33EP64MC202	70	28	64	8	4	4	4	6 Ch	1	3	1, 6 Ch	2
dsPIC33EP64MC204	70	44	64	8	4	4	4	6 Ch	1	3	1, 9 Ch	2
dsPIC33EP64MC206	70	64	64	8	4	4	4	6 Ch	1	3	1, 16 Ch	2
dsPIC33FJ32MC101	16	20	32	2	0	3	2	6 Ch	0	0	1, 4 Ch	1
dsPIC33FJ32MC102	16	28, 36	32	2	0	3	2	6 Ch	0	0	1, 8 Ch	1
dsPIC33FJ32MC104	16	44	32	2	0	3	2	6 Ch	0	0	1, 14 Ch	1
dsPIC33FJ16MC101	16	20	16	1	0	3	2	6 Ch	0	0	1, 4 Ch	1
dsPIC33FJ16MC102	16	28, 36	16	1	0	3	2	6 Ch	0	0	1, 6 Ch	1

Digital Power and Lighting

16-bit Digital Power and Lighting Products

- High performance core with DSP instructions
 - High speed control loop execution for demanding power conversion applications
 - dsPIC DSC enables low-latency control loops
- High resolution PWMs for digital power
 - Very precise duty cycle resolution of 1ns
 - Flexibility to control numerous power topologies
- Optimized digital power conversion ADC
 - Hardware triggered for precision sampling and low CPU overhead
- Complete reference designs & algorithms
 - AC/DC converter meeting platinum specification
 - LLC resonant DC/DC converter
 - Quarter brick DC/DC converter
 - Solar micro inverter
 - Interleaved power factor correction



Webinar Topics

- Building a dsPIC DSC SMPS System
- SMPS Components and Their Effects on System Design
- Control System Design for Power Converters
- SMPS Topologies: The Buck Converter
- Switch Mode Power Supply Topologies: The Forward Converter

Software and App Notes

Application Solution	AN #	Description
Switch Mode Power Supply (SMPS) Topologies (Part I)	AN1114	This application note explains the basics of different types of SMPS topologies and their applications. The pros and cons of different SMPS topologies are also explained to guide the user to select an appropriate topology for a given application, while providing useful information regarding selection of components for a given SMPS design.
Switch Mode Power Supply (SMPS) Topologies (Part II)	AN1207	This application note is the second of a two-part series on Switch Mode Power Supply (SMPS) topologies. This series expands on the previous material in Part I, and presents the basic tools needed to design a power converter.
Offline UPS Reference Design	AN1279	The application note describes the design of an Offline Uninterruptible Power Supply (UPS) using a Switch Mode Power Supply (SMPS) dsPIC Digital Signal Controller (DSC).
Digital Power Interleaved PFC Reference Design	AN1278	The application note describes the design of a Digital Power Interleaved PFC (IPFC) using a Switch Mode Power Supply (SMPS) dsPIC Digital Signal Controller (DSC).
Quarter Brick DC-DC Reference Design	AN1335	This application note describes the design of Quarter Brick DC-DC Reference Design using Switch Mode Power Supply (SMPS) dsPIC Digital Signal Controller(DSC)
DC-DC LLC Resonant Converter Reference Design	AN1336	This application note describes the design of DC-DC LLC Resonant Converter Reference Design using Switch Mode Power Supply (SMPS) dsPIC Digital Signal Controller(DSC)
Grid Connected Solar Microinverter	AN1338	This application note describes the design of Grid Connected Solar Microinverter Reference Design using Switch Mode Power Supply (SMPS) dsPIC Digital Signal Controller(DSC)
Class B Safety Software Library for PIC® MCUs and dsPIC DSCs	AN1229	This application note describes the Class B Safety Software Library routines that detect the occurrence of Faults in a single channel CPU. These routines have been developed in accordance with the IEC 60730 standard to support the Class B certification process.

Featured Digital Power Products

Product	Pins	Flash (KB)	RAM (Bytes)	IC/OC	PS PWM	ADC	Analog Compare	UART/I ² C™/SPI	CAN
dsPIC33FJ06GS001	18	6	256	0/0	4	6 Ch, 2 S&H	2	0/1/0	0
dsPIC33FJ09GS302	28	9	1K	1/1	6	8 Ch, 3 S&H	2	1/1/1	0
dsPIC33FJ16GS504	44	16	2K	2/2	8	12 Ch, 6 S&H	4	1/1/1	0
dsPIC33FJ32GS406	64	32	4K	4/4	12	16 Ch, 5 S&H	0	2/2/2	0
dsPIC33FJ64GS606	64	64	9K	4/4	12	16 Ch, 5 S&H	4	2/2/2	1
dsPIC33FJ64GS610	100	64	9K	4/4	18	24 Ch, 6 S&H	4	2/2/2	1

Connectivity for PIC24 MCU & dsPIC DSC Families



Ethernet



CAN



Microchip offers support for a variety of wired and wireless communication protocols, including peripheral devices and solutions that are integrated with a microcontroller or digital signal controller. Many of these communication libraries are integrated into the Microchip Libraries for Applications (MLA) which can be downloaded at www.microchip.com/MLA. This includes software libraries, drivers and demo code. Additional software libraries are listed at www.microchip.com/libraries.

USB

There are many PIC24 MCU and dsPIC DSC families with integrated USB which include support for device, host and On-The-Go functionality. These products are supported by the PIC24F Starter Kit (DM240011), dsPIC DSC USB Starter Kit (DM330012) as well as the Explorer 16 Board (DM240001) with USB PICtail Plus Daughter Card (AC164131).

Microchip's free USB framework includes USB software libraries as well as a comprehensive set of host and device drivers including Human Interface Device (HID) class for user interfaces, and Mass Storage Device (MSD) class for memory devices as well as CDC, PHDC, Customer, Audio, Printer and demo code including thumb drive bootloader, and printer host. The USB libraries, drivers and demo code are all available with the MLA download.

Ethernet

Applications using PIC24 MCU and dsPIC DSC products often need to connect to the internet via wired or wireless capability. Any of our PIC24 MCU and dsPIC DSC products can easily be matched with the ENC624J600 100Mbps Ethernet MAC/PHY controller to add Ethernet connection. An Ethernet PICtail Plus Daughter Board (AC164132) is available to plug into the Explorer 16 (DM240001) for developing embedded Ethernet applications.

Microchip's free TCP/IP stack is also available as part of the MLA and includes modular protocol services for standard TCP/IP-based applications such as HTTP server or FTP server, and includes support for SSL, DNS, TCP and UDP.

IrDA

The IrDA standard is a highly popular, inexpensive method for providing wireless point-to-point communication. Microchip's free IrDA stack is available to support 16-bit MCUs with integrated IrDA support, enabling a cost effective wireless connection with plenty of computing power left for other tasks.

CAN & LIN

Many of the dsPIC DSCs and PIC24 products include integrated CAN functionality which is ideal for applications requiring robust communications with a high-speed, reliable industry standard protocol. Vector CANbedded™ and osCAN™ development solutions support PIC24 MCU and dsPIC DSC products with embedded CAN Controllers.

LIN support is integrated into many products for low-cost, single-wire serial communication for automotive applications.

A CAN/LIN PICtail Plus Daughter Board (AC164130-2) is available to plug into the Explorer 16 (DM240001) for developing embedded CAN or LIN applications. This must be used with a processor Plug-In Module (PIM) for a compatible PIC24 MCU or dsPIC DSC product.

Wireless

Microchip offers a wide range of wireless modules ranging from Wi-Fi®, Bluetooth®, and various Personal Area Networks. These fully-certified surface mount modules allow designers to quickly and seamlessly add wireless connectivity to their applications. For wireless sensors and other battery operated applications, the XLP PIC24 MCUs are an ideal companion to the Microchip wireless modules to run the protocol stacks and offer very long battery life.

Stacks for these wireless protocols are available for the PIC24 MCU and dsPIC DSC families including: Embedded Wi-Fi, ZigBee® and MiWi™ wireless networking protocol.

Support

Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. In addition, the following service areas are available at www.microchip.com:

- **Support** link provides a way to get questions answered fast: <http://support.microchip.com>
- **Sample** link offers evaluation samples of any Microchip device: <http://sample.microchip.com>
- **Forum** link provides access to knowledge base and peer help: <http://forum.microchip.com>
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Netherlands - Drunen

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UK - Wokingham

Tel: 44-118-921-5869

Training

If additional training interests you, then Microchip can help. We continue to expand our technical training options, offering a growing list of courses and in-depth curriculum locally, as well as significant online resources – whenever you want to use them.

- Technical Training Centers: www.microchip.com/training
- MASTERs Conferences: www.microchip.com/masters
- Worldwide Seminars: www.microchip.com/seminars
- eLearning: www.microchip.com/webseminars
- Resources from our Distribution and Third Party Partners www.microchip.com/training

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China - Qingdao

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China - Wuhan

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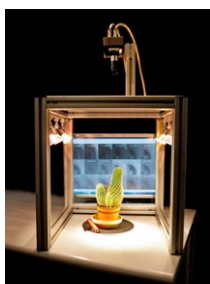
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Imec introduces hyperspectral CMOS camera for snapshot and video

imec has designed a prototype hyperspectral imager for snapshot and video acquisition. Being fast, compact and cost-efficient, the CMOS-based imaging systems comes with integrated



hyperspectral filters suited for multiple industrial vision applications. The prototype hyperspectral imager captures an entire multispectral image at one discrete point in time. The imager is achieved by applying a hyperspectral filter in a novel tiled lay-out on a commercially available CMOS-based image sensor (CMOSIS CMV2000, 2 megapixel, max 340fps).

The imager and off-the-shelf fore-optics

simultaneously duplicates the scene onto each filter tile, acquiring multispectral image cubes of 256x256 pixels over 32 bands in the spectral range of 600-1000nm at up to 340 cubes per second—compliant to normal machine vision illumination levels. Imec's line scan solution monolithically integrates hyperspectral filters on a CMOSIS CMV4000 imager (4 megapixel, max 180fps). It scans 100 spectral bands in the 600-1000nm wavelength range. The filter bandwidth (Full Width Half Max) is about 10nm across the spectral range, with a transmission efficiency of about 85%. The speed of the system corresponds to an equivalent speed of 2,000 lines per second, significantly exceeding current state-of-the-art hyperspectral sensors.

imec

www.imec.be

USB 3.0 imaging solution supports up to 100 meters of optical cable

Lumenera together with Icron Technologies have announced a joint solution to extend USB 3.0 cameras beyond the typical 20 meters of cable limitation for standard USB cables. Lumenera has addressed this issue with Icron's 100 meter multimode fiber extender system for SuperSpeed USB 3.0. Lumenera's Lt425 and Lt225 USB 3.0 cameras can be installed with Icron's USB 3.0 Spectra 3022 100 meter optical extender. The combined solution leverages the high-bandwidth USB 3.0 interface to deliver high speed, high resolution images even at distances as far as 100 meters. This plug-and-play joint solution enables new applications for USB 3.0, plus facilitates versatility. The Lt425 and Lt225 offer high-speed streaming video and image capture using SuperSpeed USB 3.0 technology to ensure the fastest image delivery, up to 170 frames/s at maximum resolution. The industry proven CMOSIS CMV4000 and CMV2000 megapixel sensors with fully electronic global shutter capture excellent quality, high-speed images with zero blur. The fully locking USB 3.0 cabling and digital interface ensure a simple plug-and-play installation with no framegrabber required. The built-in camera memory delivers a dependable, reliable flow of images, without exception. Built-in FPGA-based image processing ensures the highest image quality without having to compromise on performance. Icron's Spectra 3022 is a SuperSpeed USB 3.0 extension solution, which supports USB 3.0 5Gbps throughputs up to 100 meters via OM3 multimode fiber optic cabling.

Lumenera

www.lumenera.com

Audio codec enhances smartphone sound quality

Dialog Semiconductor plc has unveiled a ultra low power audio codec, designed to provide full range, high fidelity audio capture and playback to a variety of portable devices and audio accessories. Dialog's DA7320 audio codec features a programmable Digital Signal Processor (DSP) to offload audio software from the host processor. The use of Dialog's audio algorithms has been market proven by leading smartphone OEMs to help deliver a consistent and enhanced user experience under a wide variety of use cases. By using a multi-channel architecture that digitally mixes and routes multiple audio streams, combined with programmable N-band parametric equalisation (EQ) and Dynamic Range Compressor (DRC), Dialog's technology ensures louder and cleaner audio delivery on headphone and speaker peripherals. A psychoacoustic bass boost (PBB) can be enabled for improved perceived low frequency response for playback on low cost small form factor speakers. DA7320 is the first release in a new family of products that will be expanded to include third party branded audio software, such as noise suppression, acoustic echo cancellation and microphone beamforming. The audio codec uses a single supply voltage of just 1.6 V, has an ultra-low power consumption of 3.85mW and supports common sample rates between 8 to 96 kHz in master and slave modes. The DA7320 comes in a 64 pin BGA package with a 0.5 mm pitch. It operates from -40 to +85°C.

Dialog Semiconductor

www.dialog-semiconductor.com

Audio codec integrates single microphone noise/echo cancellation

The TC94B24WBG audio codec from Toshiba Electronics Europe is a highly integrated single microphone noise cancellation (NC) and echo cancellation (EC) solution for high-quality voice on smartphones and portable devices. The TC94B24WBG is claimed to offer design flexibility, performance, and cost benefits so OEMs can better address challenges associated with multiple microphone audio processing. Besides processing the NC/EC algorithms, the high-performance, low-power general-purpose programmable DSP in the TC94B24WBG allows customers to implement their own software in the audio codec. This helps differentiate their products from the competition. Additionally, the highly integrated TC94B24WBG includes: a 2-channel AECM interface; a 4-channel DECM interface; a battery-conserving class-G headphone amplifier; ear speaker amplifier; asynchronous sampling rate converter; a 4-channel I2S interface; an I2C/SPI interface; and audio post processing (equalizer, dynamic range controller). It provides all of the audio inputs and outputs required by mobile and telephony products. The device interfaces with the audio I/O and the application processor in smartphones and tablets. The TC94B24WBG comes equipped with two analogue and four digital microphone inputs to suit various customers' needs. However, Toshiba's unique audio processing algorithm needs just one analogue microphone to efficiently provide NC and EC simultaneously. Outstanding noise cancellation on the TC94B24WBG is achieved through a Toshiba proprietary one microphone algorithm.

Toshiba Electronics Europe

www.toshiba-components.com

Octal 12-bit ADC uses less than 80mW per channel for medical imaging

Texas Instruments has introduced an octal, 12bit, 100-MSPS analog-to-digital converter (ADC) that provides the lowest power consumption in its class for imaging and medical applications.



The ADS5295 uses less than 80 mW per channel, which diminishes board heat and power dissipation in higher-channel-density applications. It incorporates TI's digital processing block, which combines

commonly used digital functions to help improve signal-to-noise ratio (SNR) and filter harmonics while reducing output data rate for narrow-band applications. The ADS5295 can be used in phase-array architecture systems with higher channel counts, such as ultrasound, security x-ray and non-destructive testing (NDT) applications. Using only 80 mW-per-channel at 100 MSPS and eight channels, it enables designers to increase channel count without increasing power dissipation high-density applications, while still achieving a low noise of 71 decibel full scale (dBFS) SNR. The integrated digital processing block integrates commonly used digital functions, such as a low-frequency noise suppression mode, digital filtering options and programmable mapping of low-voltage differential signaling (LVDS) output pins. This lowers FPGA cost and simplifies LVDS output routing, reducing the number of printed circuit board (PCB) layers and bill of materials cost. The device also outputs data over one or two wires of LVDS pins per channel, reducing the number of interface lines. This creates a two-wire interface, which keeps the serial data rate low to further reduce FPGA cost. An evaluation module (EVM) is available to test the ADS5295 under a variety of conditions. The ADS5295 is available in an 80-pin HTQFP package.

Texas Instruments
www.ti.com

Advanced video annotation controller board

The eVAC2000 from Advanced Micro Peripherals (AMP) is a real time NTSC/PAL video overlay and video annotation controller for the PCI/104 systems. Advanced features include a high



resolution graphics accelerator, digital NTSC/PAL TV decoder, digital NTSC/PAL TV encoder and video overlay controller, all contained within a single PC104 card. Accepting up to four composite NTSC or PAL analog video inputs including video cameras,

digital video recording equipment or regular TV broadcasts, the eVAC2000 is ideal for a wide range of applications which require titles, dynamic grids or visible watermarking. The high throughput, low latency eVAC2000 uses a high performance 64bit 2D graphics accelerator combined with an 8Mbytes frame buffer to deliver rapid video graphics processing. The board could be used for multi-media displays, live video annotation or medical and industrial imaging.

Advanced Micro Peripherals
www.amp-usa.com

Robust and low-cost 'plug-and-play' digital signage system

Powered by the fanless FitPC3 computer running WireSpring's FireCast EasyStart software, the FitSignage from andersDX offers quick, easy and affordable digital signage for small numbers of screens, ranging from point-of-sale advertising and digital menu boards to trade-show signs and public safety information displays. This combination of industrial grade hardware with no moving parts and features such as auto power resume, together with easy-to-use software, enables signage systems designed for 24/7 unattended use to be set up, mounted behind a display and loaded with content in a matter of minutes, and with energy consumption as low as 10W. Supporting almost all commonly used file types for videos, pictures, news updates, web pages and live TV content, FitSignage uses simple drag-and-drop tools that allow screens to be split into zones offering different content for either viewing only or for touch interaction. Built-in templates eliminate the need for graphics skills, while pre-loaded images and stock animations, ticker tapes and RSS live feeds can be used to quickly create a professional and compelling look and feel. FitSignage is offered in 2 variations, supporting either single or dual display support, with one low, single, lifetime cost and with no recurring maintenance or upgrades costs. Content can be easily updated from a web browser.



andersDX
www.andersdx.com

RGB laser driver for head-up displays outshines LED-driven pico projectors

Maxim Integrated Products is sampling the MAX3601, a highly integrated, 8-bit RGB laser driver for pico laser projectors in automobiles. With its small size it enables sharp, pixel-perfect heads-up displays (HUD) in cars.

Compared to existing solutions, the MAX3601 excels through brighter light and lower cost. The MAX3601 drives three RGB lasers to provide a brighter light without compromising the



low power. The high intensity of the lasers project brighter, more vivid images onto the HUD to alert the driver while enhancing safety. In addition, its high integration means longer battery life, less heat build-up, and a smaller module size. Since the three laser LED drivers are combined into one single IC, the high integration of the device helps to minimize the PCB area in the cramped space behind the dashboard. No separate optics is required. With its low bias power of only 80mW and less than 1W total module power, the chip achieves excellent power efficiency and helps designers to keep heat dissipation and thermal sinking low. The chip is available in 3x3.5 mm, 42-bump WLP and 5x5mm, 40-pin TQFN packages. It is specified over the -40 °C to +105°C temperature range.

Maxim Integrated Products
www.maximintegrated.com

Bit by Bit, DRAM module testing

By Ulrich Brandt

BUILDING DRAM MEMORY modules doesn't seem to be a difficult task. The DRAM technology is well known, components are fully standardized products and the product commodity definition forces the product to be manufactured with low cost materials and assembly lines.

If there are no challenges to produce memory modules why are there differences in quality and price?

DRAM components are quite complex, although the functionality is somewhat simple. A memory component just has to store information and return it when being read. On the other hand customers require higher and higher density at the same cost. It is almost impossible to find any other electronic component which increases in capacity yet remains the same price as quickly as DRAMs or Flash components. This is accomplished by shrinking the silicon process to smaller feature sizes, each time pushing the predicted manufacturing limits further to the next generation. Where just a couple of years ago a DRAM component with a silicon die area of a few square millimeters offered Mbits of storage, it now offers up to 8 Gbit density.

We have lost some of the significance of this. On a state of the art 8GB module there are 64.000.000.000 cells, and not one of them is allowed to fail.

The negative side effects of the shrinking roadmap are smaller and smaller electrical charges being stored in the DRAM cells. The memory core operates with lower voltages, increased crosstalk and coupling to neighboring structures. The cell dielectric uses more exotic substances, textures, and aspect ratios to enhance the capacitance, and the highly interwoven cell architecture makes it more susceptible to interference than with older technology.

DRAM chip testing and sorting

DRAMs are tested multiple times. First they are tested at wafer level where the test looks for weak cells in order to replace them by redundant bits, rows, or columns. In most cases this test is executed not at target speed but with lower frequency settings, and with support by built-in self-test (BIST). The needle prober to contact multiple DRAM dies on the wafer limits the timing frequency. The most complex speed and pattern testing is performed at the packaged level. This testing is often performed at wider temperatures, where the DRAM technology is at the weaker corners. During this testing the speed grade of the DRAM chip is determined, called speed sorting. The component is also tested against known failure modes and with internal test modes to make the test as fast and effective as possible.

The optimization of the test is one of the major cost improvements and is addressed by big teams at the DRAM manufacturer.

Some DRAMs see special additional tests, while others



receive a reduced test flow. This defines if a component is suitable for industrial, automotive or consumer use. The same DRAM part number may have seen different testing depth, and the quality of DRAM components on the spot market can differ from lot to lot.

But even if you buy top quality DRAMs from the manufacturer, there is still a handicap to produce top quality modules.

As mentioned earlier, DRAMs are built with delicate technology. Exposing the DRAM component to the high temperatures of a solder process causes a lot of stress to

the cell capacitor and its dielectric. The cell capacitance and retention time of the DRAM typically degrades during the assembly process. The DRAM manufacturer covers that by applying margins to the testing. There is always a fight between increasing test margin, and a resulting higher yield loss, and the price pressure dictating to keep the margins as small as possible.

DRAM module testing

Our experience from years of module testing has shown that there are always some weak cells which pass the outgoing test at the DRAM manufacturer and degrade during assembly of the module. These cells have a reduced storage capability and they fail when operated at high temperature and with disturbing write and read patterns. The combination of temperature and noise causes weak cells to lose the information and to sporadically fail in an application.

Many module manufacturers rely on the extensive component testing by the DRAM supplier and consider a DRAM as good even after being soldered to a module PCB. Their purpose for testing modules is to detect assembly issues, not weak DRAM cells. To check if the assembly was done correctly simple tests on a module tester or in application boards is enough, and often that is all that is done.

But this neglects the degradation effects that the assembly caused to the DRAMs. To verify that no damage has been done to the DRAM components you need to perform quite power-



Fig. 1: Swissbit's high speed tester.

Ulrich Brandt is Head of Business Unit DRAM Products at Swissbit AG – www.swissbit.com - He can be reached at Ulrich.Brandt@swissbit.com

ful tests on module level and not just at room temperature, but at the specified maximum operating temperature corners or beyond, if you test with guard band.

For DRAM components the operation conditions are given as min and max case temperature. This is by default 0°C to 85°C, and for industrial operation -40°C to 95°C. The failure modes at low and high temperature are different. At low temp there are mainly internal contacts failing. At high temperature the cell retention time is the critical parameter. There is no common approach that targets both effects with one test condition. The only guarantee to verify the full functionality of the DRAM cell after assembly is to test the module both at high and low temperature.

There are two different approaches to module testing: dedicated DRAM testers or application testing. Both have their respective advantages and limitations.

A module tester has a pattern generator, parametric unit, and driver interface. The pattern generator can create address and data sequences, but is often limited to linear addressing modes. There is no possibility of creating more random sequences. On the other hand the tester is very flexible to gauge band timing and voltage levels, and is excellent for debugging. Often the tests are very synthetic and do not resemble the real operation behavior in a PC system.

This is the strength of motherboard application testing. The tests can be very similar to the real operation conditions. Fails that you see are relevant, because they occur under conditions that can equally be found during user operation.

The application test runs at target speed, and with all the noise and imperfections that differentiates a \$200 motherboard from a \$1,000,000 high speed tester.

The shortcomings of application testing

A disadvantage of pure application testing is the impossibility to change timing settings or IO voltages. There is a more hidden handicap of application testing that many are not aware of. In application testing you run the test pattern on the same system that incorporates the device under test. First of all you cannot test 100% of the memory area, since the test program and the OS reserve some memory for themselves. But what's more, the CPU has to generate the DRAM test pattern with code written in assembly language. It is not very difficult to write fast pattern that linearly walk through the memory and write and compare. But as soon as you go for complex sequences like random address pattern, using calculation intensive operation code with a lot of XOR operations, the CPU is most of the time busy

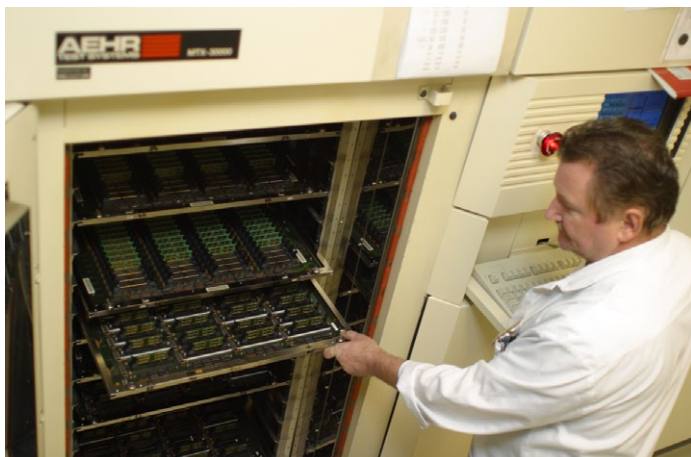


Fig. 2: Swissbit burn-in.

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+ swissbit SMemtest V4.06b (Dec 20 2012) Copyright 2012 Swissbit.

<1> Run Test
<2> Edit Test Options
<3> BIOS Memory Map
<4> Test Address Range Table
<5> SPD Bytes Table

<ESC> Exit

CPU.....Intel(R) Xeon(R) CPU E3-1225 V2 @ 3.20GHz (LGA1155)
Thread count...4/4 (used/max)
CPUSpeed/FSB...3211MHz/100MHz
BIOS.....9901 (10/08/2012)
Board.....ASUSTeK COMPUTER INC. P8C WS (HW.Rev 1.xx)
MCH.....Intel IMC IvyBridge (0xFED10000)
ECC Mode.....ECC
Total Memory...2048 (Single Channel Mode)
Timing.....1600MT/s @ 11-11-11-28 (CL-tRCD-tRP-tRAS)

Memory Controller Hub (MCH) Information available.
    
```

Fig. 3: Swissbit memory test.

to generate the next address, and not to access the memory. You need to distribute the test to multiple threads and cores to increase the band width to the DRAM module, and to test it with critical conditions. Using simultaneous multi threading (SMT) in a low level OS like DOS for memory testing is a real challenge and you need years of experience to write memory test programs that exercise the memory with critical pattern in a short test time.

If you have this expertise then multi threaded application testing with pseudo random pattern is a very effective tool to find weak cells and to guarantee top quality of a memory module.

Another hurdle to overcome in application testing is the support for ECC. This error correction can detect and correct single bit errors of memory modules, something that you want to use as an additional security against bit fails and data loss.

In a motherboard that supports ECC the memory controller permanently corrects all single bit errors that occur during testing, effectively hiding all fails from the test program. The test will report "pass" although the memory module had bit errors. This can lead to the situation that ECC modules already have undetected fails that consume most of the error correction capability of the system, rendering the ECC worthless. You need to implement support for the chipset ECC generator into your memory testing code in order to detect corrected errors and flag the module as fail.

Swissbit combines all of the best of these variables in their module testing. Each module is first tested on a dedicated memory tester, varying timings and IO voltages and measuring leakage.

And then each module is tested on a main board with a high performance proprietary memory test that causes maximum cell disturbance and long access pauses in order to drain weak cells and isolate DRAM components that may fail in customer applications at critical high temperatures. All ECC modules are fully supported and 100% tested.

For modules with industrial temperature grade Swissbit tests each individual module at -40° and higher than 95°C in order to address both low and high temp failure mechanisms. Each module has been verified at the temperature corners to cover insufficient testing by the DRAM manufacturer and the degradation during the assembly process. With this intensive testing Swissbit guarantees the highest quality, which makes a big difference with modules that have just seen a quick test after assembly.

From ROM to Flash for added flexibility

By Björn Scharfen

RESTRICTIONS OF ROM-BASED technology require new memory concepts. Until now, data were saved on a chip card with security controllers based on ROM and EEPROM memory technology. However, conventional Mask ROM technology is approaching its limits. Miniaturization of chip structures results in disproportionately increased mask costs. Furthermore, Mask ROM technology does no longer meet market requirements with regards to increasingly differentiated smart card functionalities.

On the other hand, Flash products offer a shorter time-to-market by avoiding process time in the semiconductor production. In addition Flash products allow product customization to happen at a later stage in the value chain, i.e. card manufacturers can decide prior to shipment of the card which operating system and application code to be programmed into the Flash devices depending on the project and market requirements. This offers a significant higher flexibility compared to ROM mask products, whereas typically each project requires a specific mask and the total production process down to the semiconductor fabric needs to be carefully planned.

With its Solid Flash security controllers, Infineon Technologies combines the advantages of a flexible and reliable Embedded Flash technology with high performance and certified security for the use in contact-based or contactless chip card applications. Solid Flash therefore combines the more flexible Flash memory technology with a sophisticated security mechanism that may be even superior to those of Mask ROM products. Whereas it takes several weeks with ROM products to apply a new code it can be done immediately with Solid Flash products and no compromises needs to be made on security.

NVM cell used for Solid Flash

The current Flash memory used at Infineon is based on the UCP (Uniform Channel Program) concept and has been in use for almost 10 years, proven in safety-critical automotive and SIM card applications. In smart card generations down to the 130nm node, it was mainly used in combination with ROM: ROM for the code storage and UCP initially replaced the outdated EEPROM concepts for storage of the data. For Solid Flash products in 90nm the UCP concept is also used for code storage, combining the benefits of Flash and EEPROM in one technology. The small cell size allows an economical implementation and specially contactless or dual Interface cards benefit from the fast cell access and the low power consumption.

The way from masked ROM to Flash

Historically commercial reasons demanded for a mix of ROM and EEPROM technology in smart card products. Even 10 years ago a footprint ratio of about 4:1 per stored bit led to a configuration of 4kB EEPROM and 80kB of ROM for a typical controller in payment applications. Thus, the combination of ROM to store constant program code and EEPROM for application data has yielded a cost effective combination of both technologies in smart cards. With the introduction of smaller technology nodes, the area footprint of Flash has reduced considerably to a point whereby the total cost of ownership for a ROM in comparison with Flash has to be carefully analyzed. The costs for ROM masks significantly increase with every smaller technology step of silicon geometry, e.g for a 65nm technology they are over 10 times higher than with a 220nm process. In addition, as the size of the chip gets smaller and the wafer size increases towards 300mm, the minimum order quantities of a customer specific ROM mask product of a smaller geometry chips on a larger wafer will increase to a non-economical figure and go up to a million of pieces per lot. The threshold where it does make sense to move towards Flash depends on the overall memory size as well as on the chip size. In other applications such as automotive and security controller for SIM Cards this threshold

Dipl.-Wirtsch.-Ing. (FH) Björn Scharfen, Marketing Director, is heading the product marketing and management of the Secure Mobile & Transaction Business Line at Infineon – www.infineon.com



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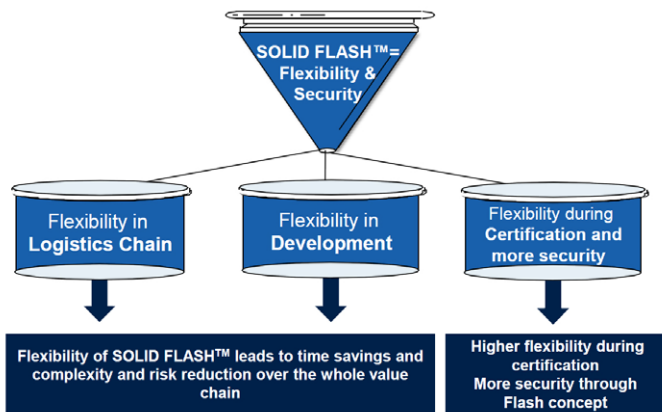


Fig. 1: Solid Flash provides several advantages for logistics and development.

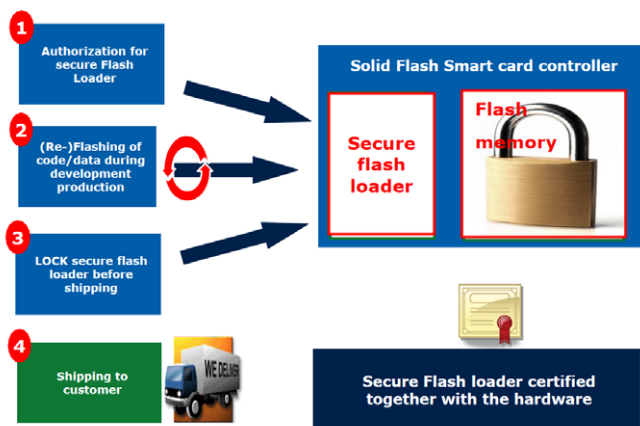


Fig. 2: Principle of the secure Flash loader.

has been reached already years ago, for the remaining smart card applications Solid Flash products were developed.

Infineon already had its first Flash based security controller EAL5+ high certified in 2006. All platforms from 90nm onwards are planned without customer ROMs in favour of Flash. In the meantime all required certifications (CC EAL 5+/6+ (high), EMVCo, several local type approvals around the world) have been obtained. Replacing ROM with Flash certainly is a paradigm shift for the industry for secure applications. But, with respect to applications and security there is no difference between ROM and Solid Flash based products. Principally the only difference lies in the fact that the locking of the code has been moved from the ROM mask creation in the semiconductor production towards the (pre-)personalization phase which also has to be done in a secure and certified environment.

Security mechanisms

The high functional security of Solid Flash is achieved by a secure mask transfer equal to that of a ROM mask code, secure and encrypted downloading and a special blocking mechanism. The program code of Flash products must be protected after programming to be secured against changes in the field. Moreover every Flash-based security

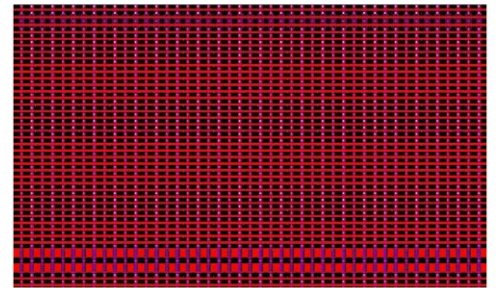
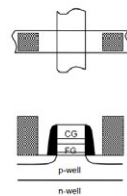


Fig. 3 All Solid Flash products are based on the same UCP cell.

chip has a chip-specific random key for encryption, whereas for mask ROM all chips that belong to the same ROM mask (often millions) have the same key.

Given the fact that Flash products offer the flexibility to download the Card Operating System and the applications into the smart cards during development and the production phase, it is not only necessary to protect the access to the secure loading mechanism by a project- and customer-specific key but it is also crucial to permanently deactivate the mechanism before deployment. This is to prevent any attacker from using the secure loading mechanism to download malicious applets to carry out attacks against the chip. The Solid Flash products provide a certified locking mechanism, which protects the programmed memory content after personalization to the same level like in ROM products. The mechanism is part of the specific Flash loader from Infineon, which is certified together with the hardware by Common Criteria, EMVCo and other type approvals. Also provisions in the hardware architecture to protect the memory from analysis and manipulation have been made.

Storage of information in Flash cells offers another advantage if the chip is subject to reverse engineering. In ROM products, the information is typically stored in metal conductors, so that the ROM content itself can be read by relatively simple means. Flash memory cells, in contrast, store the information as electrons only, making reverse engineering more difficult. In Solid Flash products a hardware firewall is implemented in order to separate code, data and other applications. This provides ef-

Memory	Description	Characteristics	+ Advantage - Disadvantage
ROM	Read Only Memory	Content is "written" only once during chip manufacturing; mainly used for program code	+ Small area footprint - Low logistics flexibility (application-specific chip production) - No writing possible + High reliability (hardwired code/data)
NVM	Non Volatile Memory	Generic term for memory technologies that store content after power-off; freely usable for code and application data (i.e., EEPROM, FLASH, UCP, etc. are all NVM memories)	
EEPROM	Electrical Erasable Programmable Read Only Memory	Implementation of NVM with small write granularity/page size, mainly used for data but also utilized for code patches	- Large area footprint + High logistics flexibility + Fine write granularity
FLASH	FLASH Memory	Implementation of NVM with larger write granularity/page size compared to EEPROM; mainly used for code, and in combination with EEPROM emulation mechanism also suitable for data	+ Small area footprint + High logistics flexibility - Coarse write granularity
IFX NVM	Infineon NVM technology based on Unified Channel Programming (UCP)	FLASH concept utilized by Infineon in combination with EEPROM emulation implemented in hardware; freely usable for code and data	+ Small area footprint + High logistics flexibility + Highest reliability due to sophisticated hardware mechanism
SOLID FLASH™	Infineon Trademark for secure & reliable FLASH products	Infineon FLASH concept with sophisticated security concept; freely usable for code and data	+ Same security and reliability as standard Flash concept + Additional security mechanism including write protection

Table 1: Comparison of storage technologies for smartcard products.

efficient protection from unwanted or unauthorized manipulation of the memory content. In order to provide the code and data in security-certified products with the best possible protection, the memory is also encrypted.

The logistics chain is also a constituent of the certification process with appropriate security specifications, similarly to ROM products. Well thought-out error recording and error correction provides extremely good reliability with regard to the memory content. Depending on the use case data retention of up to 20 years can therefore be achieved.

Scalable solutions

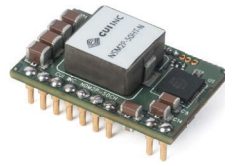
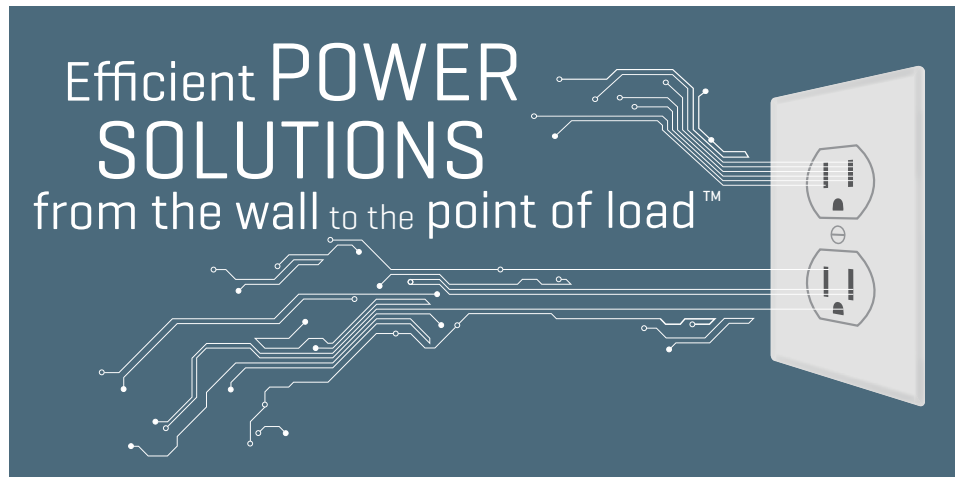
A wide range of Solid Flash ICs of different product families (SLE 77, SLE 78, SLE 97) are available and are shipped as contact based, contactless (CL) and dual interface (DIF) products. The members of the SLE 77 family are designed for contact-based and contactless SDA and DDA payment product. The high performance 16-bit controllers, with excellent characteristics also in CL DIF products are available for mass-market applications with Flash memories of 80 to 240 KBytes, with appropriate EMVCo and common criteria certifications up to CC EAL5+ (high). The 16-bit controllers of the SLE 78 family with Solid Flash variants with up to 500 KBytes provide a simple migration path from the SLE 77, and are additionally equipped with the "Integrity Guard" digital security technology. This security technology includes a dual CPU implementation for error detection; encrypted calculation in the CPU, memory, bus and cache; Error Detection Codes (EDC) for all memories, Error Codes for cache protection and active I2 shielding protection.

Thanks to Integrity Guard the security controllers are able to monitor the entire data path continuously by means of complete error detection. The SLE 78 security controllers have two CPUs, with which error detection is even possible during data processing. If the security controller detects an error or an attempted attack, it decides whether the computing operation is continued or an alarm is triggered and the computing operation is automatically aborted. The entire data path of a chip card controller is also encrypted. The encrypted calculation in both CPUs is a unique feature.

The 32-bit controllers of the SLE 97 family provide a modular concept for high-end applications such as SWP based NFC and High-End SIM/ UICC, Mobile Payment and embedded security. The product family is based on the ARM SC300 architecture but is optimized to fit to the addressed security applications, e.g. with a cache and dedicated security features.

Security in encrypted ROM	Security in encrypted Solid Flash
Mask specific ROM key	Chip specific random key - NVM key generated on-chip during personalization
Read out protection by mask individual encrypted memory content	Read out protection by chip individual encrypted memory content
Encrypted Bits stored in metal connections	Encrypted Bits stored in Floating Gates - more difficult for reverse-engineering
Error Code Protection against manipulation attacks	Error Code Protection and dynamic storage location scrambling against manipulation attack

Table 2: Comparison of security in encrypted ROM and encrypted Solid Flash.



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Moving from magnetic random access memory to magnetic logic units

By Bruno Mussard

Magnetic random access memory (MRAM) is a new non-volatile memory technology that is growing in acceptance as a mainstream technology for data storage. It integrates a magneto-resistive device with a silicon-based selection matrix. The key attributes of MRAM are its non-volatility, its low voltage operation, an unlimited read and write endurance, fast read and write operation and ease of integration as back-end technology. These characteristics give MRAM the potential to replace many types of memory in various applications.

In its most simple implementation an MRAM cell is composed of a magnetic tunnel junction (MTJ) connected to a select transistor. An MTJ is composed of two magnetic layers separated by a thin oxide tunnel barrier. One magnetic layer has a fixed magnetic orientation and is called the reference layer (FR), the other layer called storage layer (SL) has an orientation that can be switched from one direction to the other. The resistance of the memory bit is either low or high depending on the relative magnetic orientations of storage layer to a fixed reference layer, either parallel or anti-parallel. To read one bit, the select transistor is turned on, and a small read current flows through the tunnel junction as shown in figure 1. The value of the junction resistance is then compared to a reference resistance half-way between the high and low resistance values.

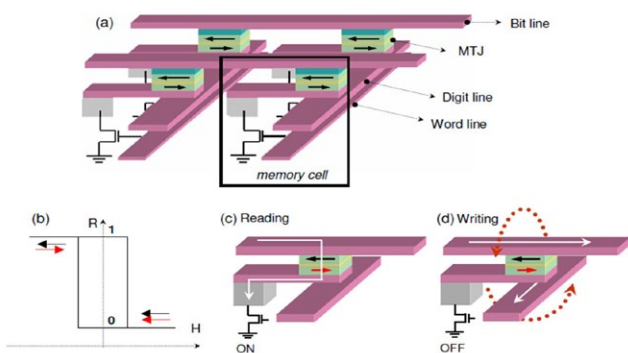


Fig. 1 : (a) Conventional architecture used in the first MRAM generation containing MTJ cells at the intersection of orthogonal writing lines and on top of a selection transistor. (b) Schematic view of a minor hysteresis loop showing the reversal of the storage layer and two corresponding resistance levels : high "1" and low "0". Reading (c) and writing schemes (d) used in the conventional MRAM architecture. At read, the selection transistor is ON and a small electric current flows through the MTJ stack, allowing its resistance measurement. At write, the selection transistor is OFF and the combination of 2 orthogonal magnetic fields ensures the selectivity.

Bruno Mussard is Security BU Technical Leader at Crocus Technology – www.crocus-technology.com – He can be reached at bmussard@crocus-technology.com

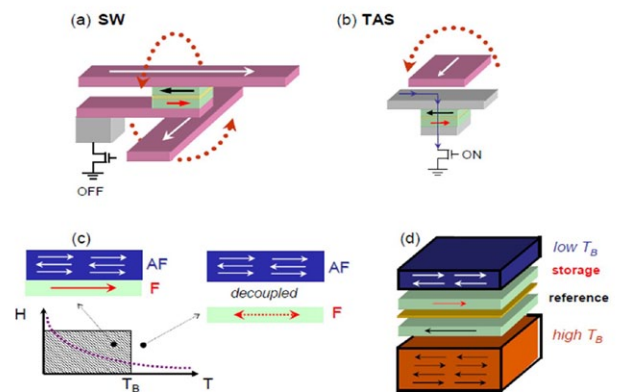


Fig. 2 : The Writing procedure in a conventional MRAM architecture (a) and in the TAS-MRAM architecture (b). In the TAS –MRAM writing approach (c), the memory cell write is possible only after overcoming the blocking temperature of the antiferromagnet which pins the storage layer (when the 2 layers are magnetically decoupled). (d) General view of a TA-MRAM stack with both the storage and the reference layer pinned with antiferromagnetic layers.

Different MRAMs have been proposed that distinguish themselves mainly by the method used to write the storage layer.

A problem, common to all these traditional approaches, is their scalability. As the MTJ is reduced in size, its ability to retain a written data state over time is also reduced. Various methods have been used to counteract this effect but they all imply using much higher powers to write the data making the memory unattractive from an application point of view thus limiting their market penetration.

The TAS-MRAM concept

To break this vicious circle of low power writability versus data retention, a new approach was proposed called Thermally Assisted Switching (TAS-MRAM). This simple approach uses temperature to differentiate between the properties required for data storage and those require for low writing power. In the TAS-MRAM scheme invented at the CEA/Spintec Laboratory, the magnetic storage layer is modified by adding an antiferromagnetic layer that essentially "blocks" the storage layer's orientation during read operations. The write process shown in figure 2 then consists of locally heating the junction to a temperature high enough to disable this "blocking" property thus allowing the storage layer to be re-oriented in a low magnetic field. This scheme thus enables a fully scalable bit cell, low power writing and excellent data retention.

From MRAM to Magnetic Logic Unit (MLU)

The exceptional stability of the stored information obtained using the TAS-MRAM concept has enabled Crocus Technology to develop a new concept called Magnetic Logic Unit (MLU). At the heart of the MLU is a self-referenced (SR) magnetic cell that

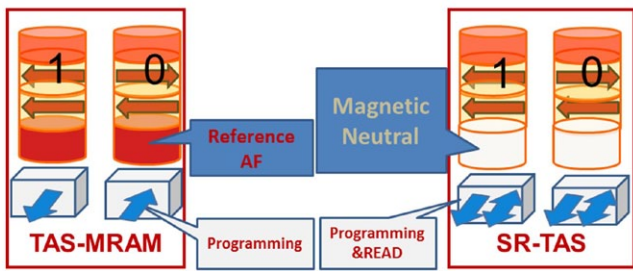


Fig. 3: TAS-MRAM with fixed reference (FR) vs SR-TAS with sense reference (SR).

is achieved by simply replacing the fixed reference layer (FR) with a magnetically free layer renamed as the sense layer – see figure 3. As before the resistance of the SR bit cell depends on whether magnetic orientations of the sense and storage layers are parallel or anti-parallel. However, since the sense layer orientation can be controlled using the field line, it becomes a true 3-terminal logic element where the output value is a comparison between the stored data orientation and that of the sense layer defined by the input to the field line. This element acts as an XOR (exclusive OR) logic device.

This now allows magnetic elements to be arranged in chains giving NAND type architectures (Lcell) in addition to the traditional NOR memory architectures. In memory applications a differential read is used where the sense layer is switched during read. Only the sign of resistance change defines the stored data state and an external reference resistance level is no longer required. The MLU enables not only rugged and fully scalable memory solutions but also enables new secure functions such as Match-in-Place that are simply not possible with traditional “memory only” architectures.

Match in place

Crocus Technology has developed an innovative function called Match-in-Place to authenticate users without exposing any confidential data to a security attacker.

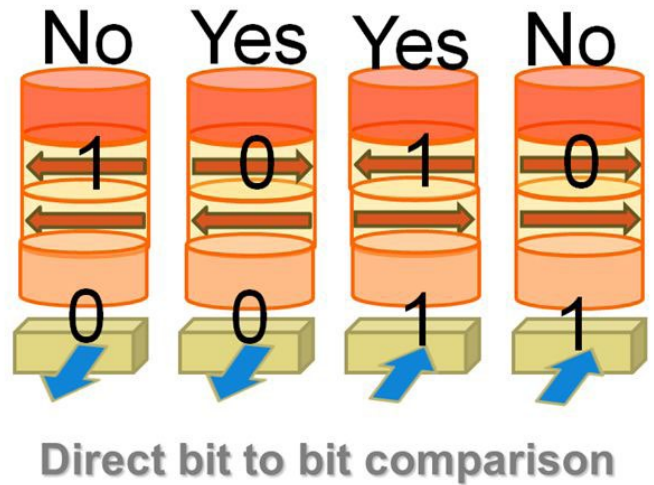


Fig. 4: Match in Place.

Each cell of the Match-in-Place architecture is a non-volatile memory cell combined with the virtual XOR gate of the MLU. Multiple cells are connected in series to create a NAND chain in which confidential data is stored. User data is then applied to the field lines and the resulting chain resistance is either correct or incorrect. If the input data is incorrect (ie does not match with stored data), no information leaves the memory and an information is available as to which bits are incorrect. This is the basis of a linear Match-in-Place engine. If multiple Match-in-Place NAND chains are placed in parallel, they can act in the same time to compare one pattern against many stored patterns.

In example of figure 4, a set of 4 MLU cells are connected serially and form a NAND chain that create a linear Match-In-Place engine. The input binary pattern 0011 is compared to the stored binary pattern 1010. Each stored bit is individually compared to the bit of the same rank. The sensitive stored data are never read and exposed to the attacker, the matching cycles can be orders of magnitude more efficient than existing solution in term of speed and power. Match-in-Place engines



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could act as a hardware accelerator, simplify the IC architecture and reduce its overall price. Fields of application for this new architecture are quite wide and include secure microcontrollers, biometric devices and associative memory devices.

Use case: secure microcontrollers

Crocus has decided to focus on the security business with the development of a high-end secure product family for smart card and embedded microcontrollers. Adding Crocus' MLU function to the smart card business will give several major advantages including a shorter programming time, easier software development, reliability improvement and a faster personalization time.

Compared to existing NOR flash technology, non-volatile memory can be written in a very short time. Programming time can be as little as 60ns, which speeds up critical write operations around PIN code and keys management. Due to the inher-

ent architecture of the MLU, instruction and data can be written and erased by byte, half-word or word. No page or bank management is necessary. At advanced technology nodes, classic NVMs require complex controllers to handle functions such as wear levelling which are not necessary with MLU technology due to its intrinsically high endurance.

One of the important aspects of a smart card product is the need to personalize the programmed information, secure operating system or embedded applications to reflect issuer configurations and end-user profiles.

Fast programming thus allows significant cost reduction. The MLU-based family of secure microcontrollers from Crocus Technology features a 32-bit secure-core, MLU for Code and Data and contact and contactless interfaces. The very high-end CT32MLU1200 targets EMVco and Common Criteria EAL5+ certification

Hybrid Memory Cube gen 2 on track to support a total cube bandwidth of 160GB/s

By Julien Happich

LAST SUMMER, the Hybrid Memory Cube Consortium (HMCC), led by Micron Technology and Samsung Electronics had released the initial draft of the Hybrid Memory Cube (HMC) interface specification, consisting mainly of an interface protocol and short-reach interconnection across physical layers (PHYs). The specification still needs to be refined for very short-reach PHYs for applications requiring tightly coupled or close proximity memory support for FPGAs, ASICs and ASSPs. While the Gen 1 program was a technology demonstration running at just under 128GB/s bandwidth (over 6x what is expected of DDR4 and 15x the performance of a DDR3 module), it was a first step in proving the stacked memory-on-logic concept using a proprietary Through Silicon Via (TSV) process - see figure 1.

By stacking 4 DRAM dies vertically, each one configured as a 16-slice device - see figure 2 - with an independent I/O port for

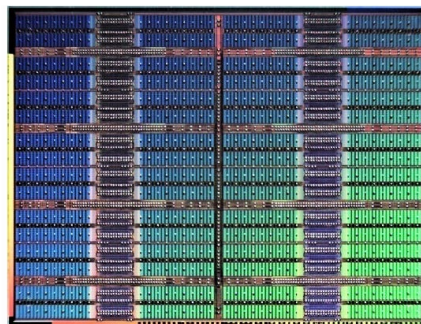


Fig. 2: One of the four 16-slice DRAM dies stacked in the Hybrid Memory Cube Gen 1.

each slice, the bottom logic die gets TSV access to all 64 DRAM slices in the stack. With two banks on each slice of the HMC Gen 1 device, this gives users a direct memory access to 128 banks, hence much shorter access latencies. The Gen 2 commercial device for which samples are expected in the second half of this year will use a similar DRAM construction and run SerDes links at up to 15Gbs, for a total cube bandwidth of 160GB/s.

"The Gen 2 specifications look rock-solid and the HMC Gen 2 device is rapidly approaching final silicon" commented Dean

Klein, Vice President of Memory System Development at Micron Technology. Already looking at Gen 3, Klein mentioned his target, to double the performance of Gen 2 no less. At this stage, without silicon, Micron is characterizing the energy performance (per bit) of the memory devices on simulated parts. Gen 2 has been characterized at about 15.6pJ/bit, that's half the energy consumption of DDR4 and under a quarter of typical DDR3 energy/bit consumption.

"One important aspect of adopting the HMC memory interface is that it will require changes to be made on the processor side, with more SerDes needed" explained Klein. "Companies have already shown their commitments to the technology, and we are a bit in a chicken & egg situation as for the processors that would support such memories. Some of the HMCC members are already developing IP that could readily be integrated into processors to interconnect with multiple high-speed SerDes links" he continued. "For this reason, FPGA vendors will certainly offer an easier route to integration" Klein concluded.

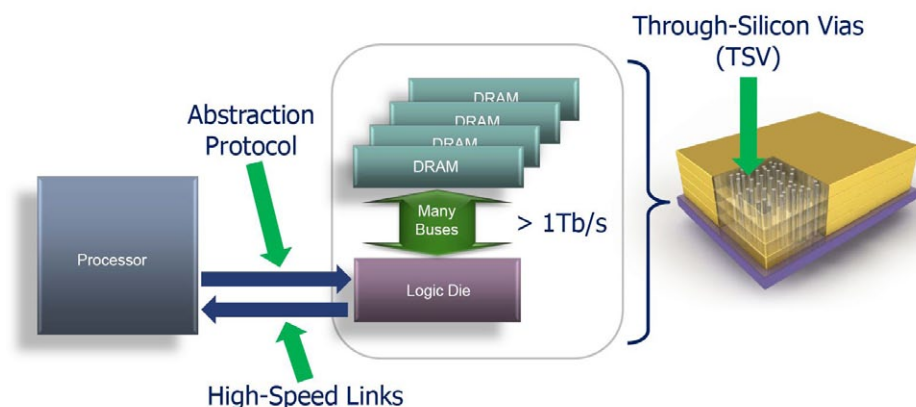


Fig. 1: The Hybrid Memory Cube concept, several DRAM dies stacked vertically on top of a logic interposer.

2TB SSD drives with a standard 2.5" SATA interface, only 9.5mm thick

Foremay has released 2TeraByte SSD drives with a standard 2.5" SATA interface and a thickness of 9.5mm. The drives are offered in the company's SC199 (for mission-critical applications) and TC166 (for terminal computing) product families. Users can opt for either industrial or commercial grade to suit their specific application. Claimed to be the largest SSD in the world offered in the standard 2.5" SATA form factor, the unit features integrated flash management technologies such as self-monitoring analysis and reporting technology, advanced power management and advanced error correction algorithm. It also provides optional features such as fast erase, military secure erase methods, hardware based encryption and conformal coating.

Foremay
www.foremay.net



Re-programmable 256-bit transistor-based and 1-kbit diode-based non-volatile memory

The EU-funded eMbedded Organic Memory Arrays (MOMA) project has announced the largest re-programmable non-volatile memory arrays yet produced on flexible substrates.



Its 256-bit transistor-based and 1-kbit diode-based arrays exhibit state-of-the-art performance in numerous key memory parameters, plus excellent production yields, according to the project team. The MOMA consortium brings together commercial

and research partners from across the memory value chain. These partners are chip maker STMicroelectronics, materials supplier Solvay Specialty Polymers, innovation centers imec and Holst Centre plus Catholic University of Louvain and University of Groningen. The project focuses on ferroelectric memories based on soluble ferroelectric polymers and organic and oxide semiconductors. It has successfully developed new grades of memory materials that can be tailored to specific applications and deposition techniques (including spin-coating, inkjet printing and imprinting). The project partners used these materials to develop memory arrays based on both transistors and diodes, optimizing production processes to deliver high yields and excellent memory performance. With its 1-kbit (32x32) array, MOMA has delivered the largest flexible memory arrays to date and achieved production yields close to 100%. Furthermore, it has created the thin-film read-out electronics necessary for use in real applications. In the remaining months of the project, the partners will combine all these building blocks into a 96-bit array with the related read/write circuitry, creating a complete embedded flexible memory suitable for applications such as Electronic Product Code (EPC) tags. The project partners are now looking for interested parties to cooperate on further development and commercialization of the technology.

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EEMBC to develop Ultra-Low Power microcontroller benchmarks

By Nick Flaherty

THE EMBEDDED MICROPROCESSOR Benchmark Consortium (EEMBC) has set up a working group to develop a standardized, industry-endorsed method to evaluate the energy efficiency of ultra-low power (ULP) microcontrollers. To date, the industry has lacked a common method to test, validate, and compare the real-world energy consumption of these Microcontrollers that target applications such as portable medical devices, security systems, building automation, smart metering, and also applications using energy harvesting devices.

The new benchmark will initially look at the power used when a controller moves from running to its real time clock sleep mode. New benchmarking code will be required as the standard CoreMark benchmarks use too much power, says Horst Diewald, chief architect of MSP430 Microcontrollers at Texas Instruments (TI) in Germany who is chair of the EEMBC ULP working group. "We have seen a significant need for a well-constructed, industry-accepted benchmark to equitably evaluate the energy efficiency of microcontrollers," said Diewald. "Unfortunately, the application developer cannot rely on datasheet parameters alone to compare total Microcontroller power consumption and select an appropriate microcontroller."

The first benchmark should be available by the end of March

to assess different controllers. Members of the group include Analog Devices, ARM, Atmel, Cypress, Energy Micro, Freescale, Fujitsu, Microchip, Renesas, Silicon Labs, STMicro and TI, although some notable energy harvesting device developers are missing. Unlike other EEMBC benchmarks that endeavor to measure the top performance of processors and systems, the ULP benchmark will focus on measuring the energy consumed by Microcontrollers running various computational workloads over an extended time period. The benchmarking methodology will allow the Microcontrollers to enter into their idle or sleep modes during the majority of time when they are not executing code, thereby simulating a real-world environment where products must support battery life measured in months, years, and even decades.

"EEMBC's primary goal is to develop fair and unbiased benchmarks for the embedded industry. In support of this goal, I am very excited that the EEMBC members are so motivated to develop this much-needed ULP benchmark," said EEMBC president Markus Levy. "In the system developer's interest, we encourage all relevant companies, including the system manufacturers, Microcontroller vendors, and tool providers, to join us in this effort."

Samsung reveals eight-core mobile processor

By Peter Clarke

SAMSUNG ELECTRONICS has launched an eight-core ARM-based processor that uses the big-little processing technique announced by ARM Holdings plc in 2011. The announcement was made by Stephen Woo, Systems LSI president of the Samsung during a keynote presentation at the Consumer Electronics Show being held in Las Vegas. Woo said the Exynos 5 Octa is the world's first mobile application processor to implement the big-little processing strategy. The chip has a quad-core Cortex-A15 processor optimized for high performance and a quad-core Cortex-A7 processor that is optimized for lowest power operation.

The Exynos 5 Octa is a follow-on to the Exynos 5 Dual, which is already designed into products including the Google Chromebook and the Samsung Nexus 10 tablet. Samsung did not indicate in what manufacturing process technology the Exynos 5 Octa is implemented or the highest clock frequency or lowest voltage operation of which the chip is capable.

In a statement issued by Samsung Woo described the Exynos 5 Octa as the "best application processor currently available." It is a claim for which there is much competition. At CES Qualcomm has announced the Snapdragon 800 quad-core processor, Nvidia has announced the Tegra 4 and ST-Ericsson the NovaThor

L8580 ModAp. Both the Snapdragon and NovaThor parts have an LTE modem integrated with the application processor.

Warren East, CEO of ARM, joined Woo on stage and helped introduce the big-little technology that debuts in the Exynos 5 Octa. The application processor provides up to 70 percent higher energy efficiency than the previous quad-core Exynos.

Samsung did not disclose what process technology is being used for the Exynos 5 Octa, nor what graphics processing unit has been selected. The previous generation Exynos 4 Quad and Exynos 5 Dual are both made using 32-nm CMOS and include quad-core Mali GPUs, also licensed from ARM.

There is speculation that the Octa chip is implemented in 28-nm CMOS and that the quad-core Cortex-A15 runs at up to 1.8-GHz and the Cortex-A7 cores run at 1.2-GHz. Similarly it is thought that the GPU is the ARM Mali-T604 quad-core GPU used in the Exynos 5 Dual, with the two chips also likely to share the same 32-bit dual-channel 800MHz memory controller with its DDR3 and LPDDR3 memory support and peak 12.8GB/s bandwidth. If the Exynos 5 Dual is a guide the Octa will have a dual channel 32-bit memory interface capable of 800-MHz LPDDR3/DDR3 or 533-MHz LPDDR2 capable of 12.8-Gbyte per second and 8.5-Gbyte per second bandwidth respectively.



Industrial imaging computer features multi-core CPU, GPU and FPGA technology

Designed for computationally-demanding industrial imaging applications, the Matrox Supersight Solo high-performance computing platform from Matrox Imaging lets users integrate a powerful system host board with multiple GPUs, FPGAs and frame grabbers in a single robust chassis. Matrox Supersight Solo lets OEMs and systems integrators maximize compute density in a 4U chassis with up to thirteen PCIe 2.0 x16 slots. It also enables increased data bandwidth with dual PCIe 2.0 x16 host interfaces. The included system host board is equipped with one or two multi-core embedded Intel Xeon processors. Applications for Matrox Supersight Solo are developed using the Matrox Imaging Library (MIL), which includes tools for every step in the process: from application feasibility, to prototyping, through to development and ultimately deployment.



Matrox
www.matroximaging.com

New multicore microcontrollers create industry's largest range

XMOS has launched a new range of microcontrollers, creating what it claims is the industry's largest range of embedded multicore devices. The L Series adds 6-, 10- and 12-core variants, plus new memory size options, to the existing 8- and 16-core products in its xCORE family, which now includes over 50 devices, making it the world's broadest range of multicore Microcontrollers says the Bristol, UK-based company.

The new products join the recently announced xCORE-USB devices, and existing members of the general purpose L series (formerly known as L1 and L2). The L-series now consists of the 6-core XS1-L6-64, the 8-core XS1-L8-64 and 1000MIPS XS1-L8-128 with extended memory, the 10-core XS1-L10-128, the 12-core XS1-L12-128, and the 16-core XS1-L16-128. The new L8-128 integrates 128Kbytes of on-chip RAM and delivers enhanced performance, with each of the eight logical cores able to deliver up to 125MIPS of computing power. The introduction of 10- and 12-core options provides xCORE users with more flexibility on price and performance. The entire L-Series is organized into two pin-compatible groups, allowing designers to build multiple end-product variants using a single hardware platform, and to performance-enhance or cost-optimize designs as requirements evolve. The L-Series multicore microcontrollers are enabled by an evolution of the fundamental xCORE technology, which is based on powerful deterministic processor 'tiles', each of which is optimized to support a number of logical cores. For example, the XS1-L10-128 has two tiles, each of which provides five logical cores, giving a total of 10 logical cores in the device. Each logical core has its own instruction stream and register files, and takes a share in the tile's 64Kbytes of RAM.

XMOS
www.xmos.com

NXP and element14 team up for dual core controller development kit

NXP and element14 have joined forces on a multimedia development kit based around NXP's dual core ARM microcontroller. The LPC4357-EVB multimedia evaluation kit, exclusively available from element14, is based on NXP's dual-core LPC4357 microcontroller that combines the Cortex-M4 and Cortex-M0 processors. The high-performance, low-cost board is aimed at developing DSP and MCU applications within a single architecture and development environment. The LPC4357-EVB features 256Mbit (32 MB) of serial Flash memory from Spansion. The QSPI Flash is connected to the LPC4357's unique SPI Flash Interface which allows the M4 or M0 core to execute from the QSPI or access large tables of data or images. The Cortex-M4 processor combines the benefits of a Microcontroller with high-performance digital signal processing features such as single-cycle MAC, single instruction multiple data (SIMD) techniques, saturating arithmetic and a floating point unit. The Cortex-M0 coprocessor off-loads many of the data movement and I/O handling duties that can drain bandwidth from the Cortex-M4 core.



NXP
www.element14.com

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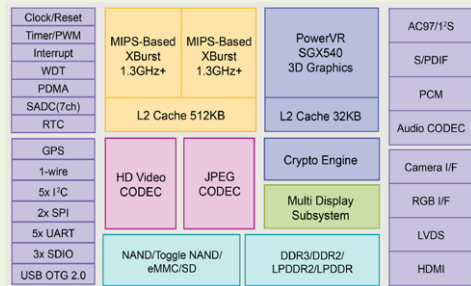


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Highly integrated MIPS dual core SoC for power-efficient affordable devices

Chinese SoC designer Ingenic Semiconductor has launched a highly integrated dual core MIPS-based SoC with PowerVR graphics in a new 10" Android 4.1 tablet reference design.



The 1.3GHz JZ4780 SoC uses Ingenic's MIPS-based XBurst processor, with an innovative high-performance and ultra-low power pipelining architecture

that consumes approximately 140mW per GHz under full load. At approximately 30mm² die size in 40nm, the JZ4780 provides a low-cost solution for consumer electronics products.

The SoC features a video processing unit (VPU) powered by a second XBurst processing engine for advanced 1080p HD video performance and includes HDMI, LVDS, audio codec, GPS baseband, and other analog/application blocks and rich interconnect interfaces plus PowerVR SGX Series5 graphics IP from UK supplier Imagination Technologies. At CES, MIPS and Ingenic showcased the JZ4780 SoC in a new 10" tablet reference design developed by Ingenic. Ingenic has also demonstrated a version of the tablet that includes embedded LTE functionality from Altair Semiconductor, with Altair's MIPS-Based FourGee chipset.

www.mips.com

Apalis: a new computer on module architecture for embedded computing

Toradex has unveiled a new, independent, computer on module architecture called Apalis, designed to be future proof and to support a range of SoCs. Interfaces on Apalis modules are divided into two categories: standard and type specific.



Standard interfaces are the ones most commonly used. These are kept entirely compatible between all modules in the emerging Apalis family. This feature

enables a price and performance optimised product with room to increase processing power and storage in the future. Type-specific interfaces such as MIPI CSI or DSI can be valuable additions, but are less commonly used in industrial applications, and usually suffer from very short product life spans in the mobile and consumer markets. Integration into custom carrier boards is made easy by Toradex's Direct Breakout technology which enables signal routing directly from the module connector to outside world I/O ports without crossing traces or traversing layers. The module can be fixed to a carrier board either with M3 screws or a MXM Snaplock connector which provides a simple retention mechanism for the development phase or in gentler conditions. The Apalis computer on module architecture comes with pre-installed operating systems - Windows Embedded Compact or Linux. First in the family, the Apalis T30 module will begin shipping in March 2013.

Toradex

www.toradex.com

Reflex CES enters mainstream FPGA-prototyping market

The FPP 25 introduced by Reflex CES is a fast ASIC/SOC prototyping platform for emulating designs of up to 25-million ASIC gates using a stand-alone system. Based on Xilinx Virtex-7 2000T FPGAs, FPP 25 exploits Reflex CES' collaboration with Flexras, an EDA company specializing in FPGA design partitioning software, and Adacsys, a functional verification software provider, to offer design engineers an easy-to-use, next generation platform to speed up validation and verification of complex, high density digital designs. FPP 25 integrates Flexras Wasga automatic partitioning design suite offering high performance partitioning, timing analysis and high speed, pin-multiplexing IP to improve design productivity. The Reflex CES FPP 25 prototyping platform can optionally add Adacsys AVA (Advanced Verification Acceleration) software for advanced verification as well as Xilinx Vivado and Xilinx ChipScope debugging tools. It operates with a GbE interface, an USB interface or a 4-lane PCIe cable (GEN2). A single platform can emulate up to 25-million ASIC gates using three high density Virtex-7 FPGAs (two XC7V2000Ts and one XC7VX485T) that are 100% available to user applications. Each Virtex-7 2000T FPGA intercommunicates by nearly 400 LVDS signals at 1.25Gbps. An onboard CPU with an embedded Linux OS is implemented to handle the configuration and monitoring functions. Up to five FPP 25 platforms can be chained together to address high density designs.



Reflex CES

www.reflexces.com

Graphic-rich embedded box PC for industrial automation applications

Aaeon's TKS-G50-QM77 is a high performance embedded box PC based on the 3rd Generation Intel Core processor. Designed for flexible customization, the TKS-G50-QM77 can easily be adopted for other applications that require high performance computing in a small form factor enclosure such as gaming, advanced digital signage, transportation and high-end kiosks.



The 3rd Generation Intel Core processors offer an overall 38% improvement over the previous generation and with a lower thermal envelope, it is a designer's choice when designing high performance, small embedded devices. The TKS-G50-QM77 includes the quad core Intel Core i7-3610QE processor with DDR3 1333/1600 SODIMM memory, and the system has a maximum of 8GB memory. TKS-G50-QM77 features two Gigabit Ethernet ports, one CRT (or DVI-I optional), 2-channel High Definition Audio, two SATA 6.0Gb/s (supports RAID 0,1 option), one CFast, two USB3.0, two USB2.0, four COM, a programmable 8-bit Digital I/O and one Mini Card expansion slot for wireless networking options. DirectX 11, OpenGL 3.1, OpenCL 1.1 and stereoscopic 3D are supported enhancing up to 50% 3D graphics performance and up to 1.8X real time HD-HD transcode improvements. The TKS-G50-QM77 is Windows 8 ready and supports most legacy embedded Operating Systems.

AAEON Technology

www.aaeon.com

AMD APU-based board for x86-based embedded systems

AMD's newly launched Gizmo board is a low-cost board geared toward x86-based embedded system development, powered by an AMD Embedded G-Series Accelerated Processing Unit (APU). Measuring 102x102mm, the Gizmo x86



development board can run a variety of operating systems including Android, Linux, RTOSes and Windows. The Gizmo board includes the G-T40E dual-core processor running at 1.0 GHz, combined on a single die with AMD Radeon HD 6250 discrete-class graphics. The board provides a performance capacity of 52 gigaFLOPS (GFLOPS) at less than 10 watts. Custom high- and low-speed edge connectors enable a full range of functions. The board offers a power-efficient foundation for high-performance multimedia content delivery.

AMD
www.amd.com

Universal Debug Engine version 4.0.2

PLS Programmierbare Logik & Systeme presents an optimized test and debugging solution, the Universal Debug Engine (UDE) version 4.0.2, for Infineon Technologies' ARM Cortex-M0



core-based 32-bit Microcontroller family XMC1000 that delivers 32-bit performance at 8-bit prices. Both the UDE 4.0.2 and PLS's Universal Access Device family seamlessly support the internal debugging resources and peripheral units of the highly integrated XMC1000 components developed for use in intelligent sensor and actuator applications, LED controls, digital power conversion, and controllers. The integrated FLASH/OTP programming functionality of the UDE guarantees maximum speeds in the whole Delete-Download-Programming-Verify cycle.

PLS GmbH
www.pls-mc.com

OpenVPX fanless embedded computer

Emerson Network Power has launched its first system-level OpenVPX fanless enclosure - including power, storage and processor elements - to minimize size, weight and power (SWaP) for high performance embedded computing applications. The VPX3000 includes a configurable I/O Adapter Board (IAB) that routes I/O from the payload blades to the front of the enclosure. The IAB is designed to mate with Emerson Network Power's iVPX7225 processor blade, based on the Intel 3rd generation Core mobile chipset. The VPX3000 accepts up to three 3U conduction cooled OpenVPX modules and includes a VITA-62 compliant AC or DC power supply with a MIL-38999 power input connector and a front panel switch.



Emerson Network Power
www.emerson.com

Prototype platform tests real-time vehicle software

With two prototyping platforms, Fraunhofer ESK is addressing the needs of software developers in the automotive industry.

The platforms enable developers to test safety-critical software-based vehicle functions in particular in the domains of infotainment and driver assistance systems. Fraunhofer's Automotive Real-Time Prototyping System (ARTiS) platform currently is available in two flavors - ARTiS-RT for real-time applications and ARTiS-XT for applications that require significantly higher computing performance. ARTiS-RT is a real-time enabled platform based on the PowerPC architecture. As a prototype ECU it can run the algorithms for vehicle control systems in electric cars and gateway applications. The product supports all common automotive data bus systems such as CAN, MOST, FlexRay and Ethernet.



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Developing and strengthening 3D IC manufacture in Europe

By Julien Happich

THE EUROPEAN 3D TSV SUMMIT that took place at Grenoble's Minattec campus late February gathered 320 attendees from over 20 countries, a testimony of Grenoble's high tech reputation and France's competitive edge in the field of 3D IC integration.

"There were only local summits so far", explained Heinz Kundert, President of SEMI Europe, "and this is truly the first time that a conference on 3D Through Silicon Vias (TSV) receives such a global attention, from key European players but also from outside Europe".

"A lot has been spent on R&D and Europe has very good universities, but we also need to maintain a critical mass in IC manufacturing in Europe, otherwise, we could lose our know-how and critical edge" continued Kundert.

There are many issues that need to be addressed for 3D IC manufacture, and now is the chance for Europe to bring IC production back from Asia, according to Kundert. "In highly automated fabs, it may no longer be economical to produce ICs in Asia, especially with all the associated costs of staff travel, and complex machine parts imports/exports", Kundert highlighted.

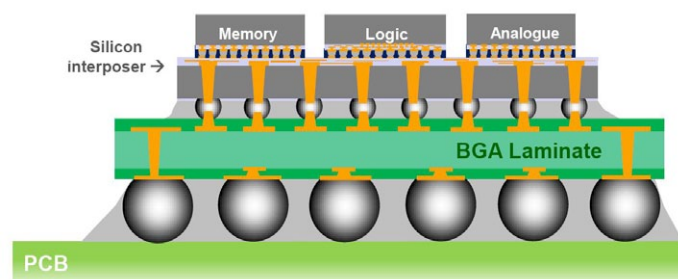
In fact, there is a reverse relocation trend happening, from Asia to Europe and to the US. As a global semiconductor industry association, SEMI Europe's role is also to ensure that its members can compete with the Asian and American industry on fair grounds, with the same sort of tax reliefs and energy deals, but also with more education in electronics.

In that sense, the European 3D TSV Summit's recent success helps raise the semiconductor industry's visibility and get the message across the European Commission. SEMI Europe documents the industry and negotiates with the European Commission on behalf of its members.

"The European Commission has now understood that semiconductors represent a key enabling technology for growth in Europe, and this needs to be supported not only with spending in R&D, but also by financing pilot production lines. We are here to raise the issues and to provide a single European strategy for the semiconductor industry, comforting our members that they have a future in Europe" concluded Kundert.

Solutions from 2.5D interposers to 3D ICs

Although the latest developments around through-silicon vias are aimed at improving direct chip-to-chip connectivity and true 3D IC designs, so-called 2.5D interposers where several chips are connected through an interposer rather than directly using TSVs still have a future. In fact in the next five years, market and technology analyst for advanced packaging at Yole Développement Lionel Cadix expects 2.5D interposers with system partitioning applications to be the biggest drivers for the volume adoption of 3D IC technology. For the global production of TSV chip wafers, the analyst forecasts an impressive compound annual growth rate (CAGR) of 56% between 2012 and 2017, with 2.5D interposer platform wafers shipping at nearly double that rate, growing from less than 100,000 12-inch equivalent wafers today to over 2.5 million in 2017. This is explained by the increasingly complex role that interposers could play in system-



A typical implementation of a system-partitioning interposer as illustrated by Yole Développement.

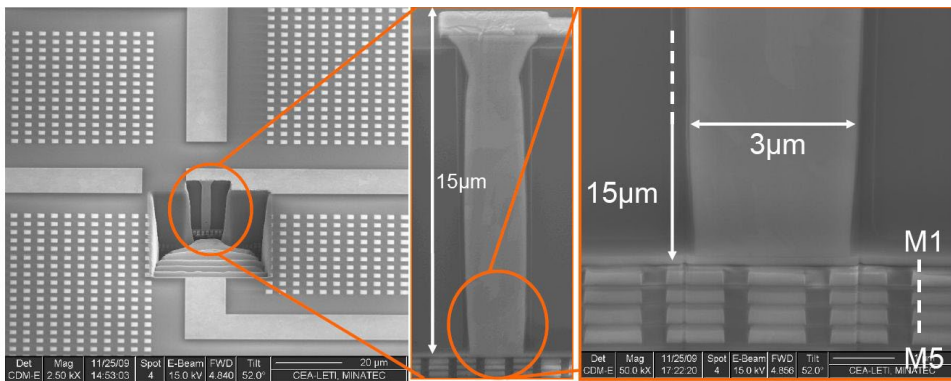
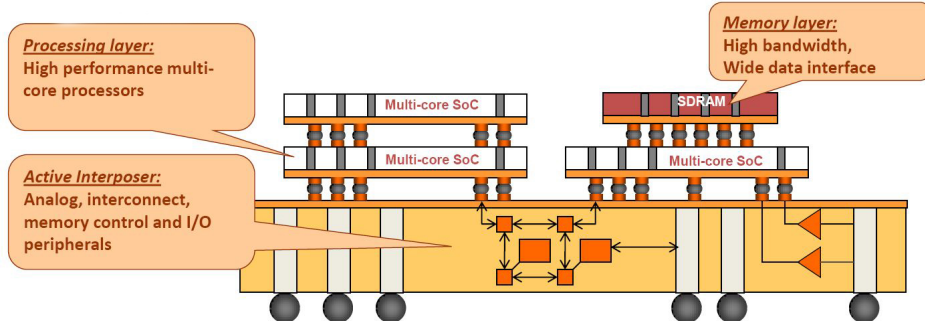
partitioning, not only enabling the integration of logic ICs with memory ICs, but possibly allowing designers to mix digital and analog ICs like in a SiP but with better electrical and thermal performances. From a thermal standpoint, 2.5D integration enables similar benefits to those of 3D integration without the thermal drawbacks of overheating, highlighted Cadix.

In such system-partitioning, the interposers can act as heat spreaders across the package surface area.

2.5D system-partitioning interposers will often offer a cost-effective alternative to all 3D IC design by enabling the use of optimised technologies for each IC (memory, logic, analog, MEMS) with higher yields. This also includes the possibility to cut down large logic chips into several circuits with higher front-end manufacturing yields. The analyst noted that beyond eight cores, processors will lose performance benefits if designed in a 2D configuration. « 2.5D interposers offer a solution to the fundamental bandwidth bottleneck of 2D architectures and will soon be mandatory for increasing the performance of high-performance computers » he concluded, taking the example of Xilinx' Virtex 7 HT (four slices processed at 28nm on a 25x31mm 100µm thick silicon interposer) or IBM's next Power 8 multi-core CPU to be based on 2.5D interposers.

According to Yole Développement, the 3D TSV market could reach USD 40B in 2017, growing more than 10 times faster than the global semiconductor industry. And 2013 could well be the turning point with the introduction of Micron's Hybrid Memory Cube.

In his presentation, CEA-Leti's CEO Laurent Malier acknowledged the importance of what he calls smart interposers, an all-encompassing expression for what could include thermal dissipation solutions, and die substrates with integrated passives, photonic interconnects or even active silicon interposers. On CEA-Leti's 2015 roadmap, the active interposer concept would support SoC partitioning into several dies, with different technology nodes. This enables the faster introduction of new processes, using small dies manufactured at a better yield. The active silicon interposer would integrate not only interconnects but also analog functions, memory control and I/O peripherals. So far, the lab has demonstrated direct face-to-back integration (wideIO memory on a SoC) and face-to-face chip integration (a logic chip on an analog one at 65nm). The ultimate goal would be to achieve modular and stackable logic dies (logic-on-logic), but this would require a 3D network-on-chip (NoC). By 2014, Malier hopes to be able to demonstrate a 3D asynchronous NoC that would support fast serial links and full asynchronous

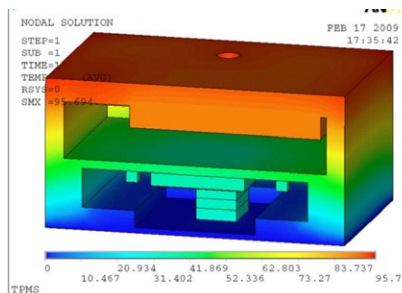


On CEA-Leti's 2015 roadmap, the active interposer and the TSV technology that must be scaled down for such solutions.

logic to avoid clock distribution issues across the stack. The network would include 2D and 3D NoC routers distributed throughout the 2D logic dies. Further on the radar, Malier also mentioned prospective work on a 3D cache memory concept to be stacked on a manycore processor. This would rely on a non-uniform memory architecture capable of splitting cache into multiple banks interconnected with a NoC. The 3D stacking would add flexibility for capacity, high bandwidth and fault tolerance. Such an architecture would require a 10µm TSV pitch and in excess of 10,000 TSVs per chip, compared to the relatively large grain 3D partitioning (50µm TSV pitch) required for logic-on-logic solutions.

Because each TSV also requires a buffer or keep-away zone (to limit unwanted capacitive couplings and mechanical stress), TSVs need to shrink to achieve surface (silicon real estate) cost reduction. Towards that goal, the lab has demonstrated high-density low diameter TSVs (3µm) across 15µm of silicon. In the future, thermal hot spots could be addressed with integrated graphite heat spreaders, but also with phase change materials for dynamic temperature smoothing, and possibly long distance heat dissipation using a cooling fluid through micro-channels.

The challenges for stacking dies into true 3D ICs are not just about process control, TSV density and 3D routing, thermal issues could become the real bottleneck. First, thermal models and design rules must be established. Xilinx' Senior Director for packaging and advanced technology development, Suresh Ramalingam shared his experience on the Virtex-7 2000T, a 2.5D device that combines a whopping 6.8B transistors across four FPGA sub-dies on a 4-layer metal Si interposer with over 10,000 inter-die connections. Ramalingam insisted on the need for co-design, optimizing dies for extra performance through homogeneous and heterogeneous 3D integration. "With 3D integration using an active die as the carrier (instead of an interposer), you have to decide which chip must go on top", he said. Ramalingam's short answer is that the high performance chip should go on top for thermal and TSV process availability (smaller diameter), whilst the bottom die, designed with a more mature technology node should support power TSVs for the top die. Again, it is critical to address the stacked thermal flux with good floor-planning. This calls for multi-physics, multi-die analysis and thermal modelling based on vertical hotspots for which the tools are yet to come, commented Uwe Knöchel, a researcher at the Fraunhofer IIS, Design



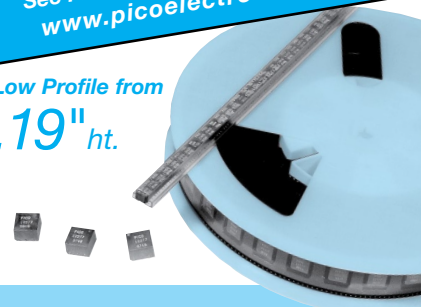
Thermal flux modelling for a 3D IC stack using Fraunhofer IIS' internal multi-physics tools.

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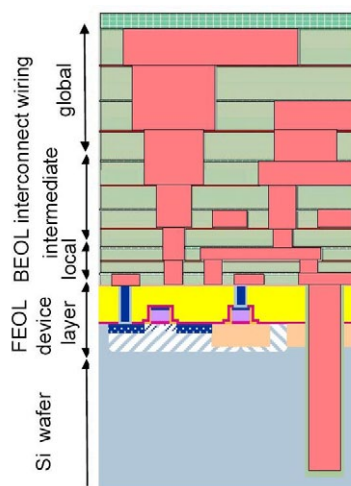
Automation Division. In fact, “3D IC stacking opens such a big design space that a new class of tools are needed to decide the best design approach. This is particularly difficult because these multi-physics, multi-scale designs exceed the capacity of current simulators”, Knöchel added. You must interface very different tools in order to achieve a thermal-aware floor-planning, for complex designs, Knöchel had to rely on in-house academic solutions.

Defining a process flow

Eric Beyne, Director of advanced packaging at imec gave us some insights on the manufacturing supply chain needed for a unified 3D IC design flow across foundries and package manufacturers. It could be split into front-end, middle-end and back-end process modules. In the front-end module where the semiconductor device structure and material patterns would be processed, a via-middle approach would consist in fabricating the TSVs after the front-end-of-line (FEOL) device fabrication, but before the back-end-of-line (BEOL) interconnects. The mid-end process module would include wafer to carrier bonding/debonding, thinning, then backside TSV reveal and passivation, and the addition of a redistribution layer, microbumps and copper pillars. The back-end process would then consist in the actual 3D stacking of the prepared dies and wafers, either die-to-die or die-to-wafer. The consensus in the industry seems to be that TSVs should be scaled down for cost and capacitance reduction. Vertically, this can be achieved by thinning the wafers and by manufacturing high aspect-ratio TSVs. Imec has demonstrated copper vias with an aspect ratio of 10 (5µm diameter, 50µm deep) obtained in a single litho-step. Further on its roadmap, the Belgium university campus sees 30µm deep TSVs with a diameter of only 2µm to be integrated with advanced device nodes. Imec has also demonstrated thin wafer handling (thinning down to 50µm) with backside passivation and copper via exposure.

An interesting contribution from Jurgen Wolf, Department Head of HDI WLP/ASSID at Fraunhofer- IZM / ASSID was to showcase the institute’s capabilities for etching TSVs with an aspect-ratio of over 12 (10µm/120µm and 5µm/60µm+) and the development of nano-

porous gold bumps for chip to substrate bonding. The new Ag/Au alloy chemistry used for bump deposition can be used in a conventional Au bumping process flow. The nano-sponge is obtained through de-alloying by wet etching the aluminium. This sponge-like gold bumps have an average pore sizes adjustable from 20nm up to 500nm and are fully compressible and able to compensate topography issues on chip and substrate, which can also be an issue for die-to-die and die-to-wafer stacking.

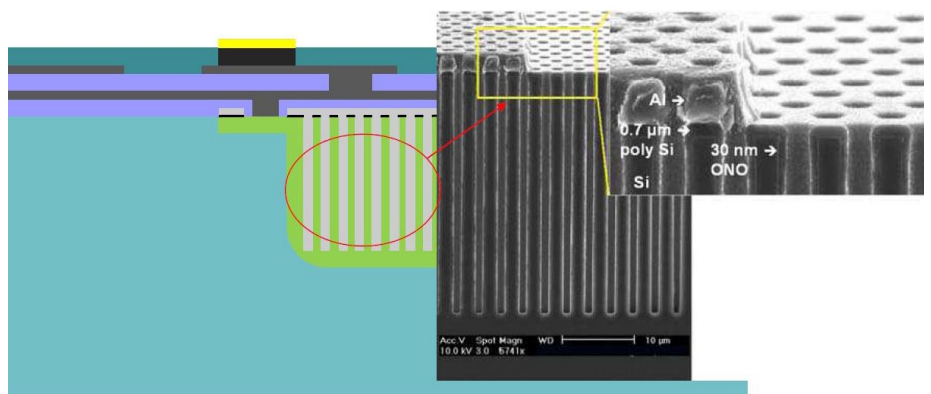
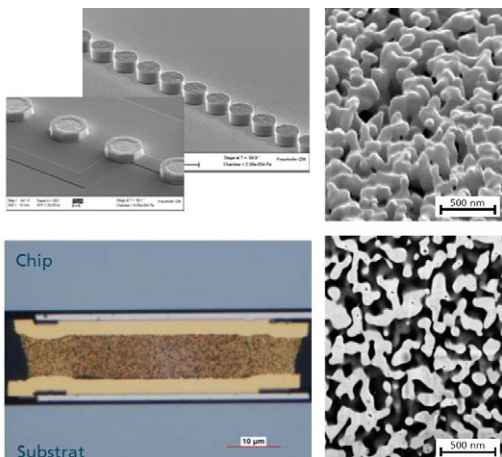


"Via-middle":
fabrication TSV's after
FEOL device
fabrication processing
but before BEOL
interconnect.

imec has demonstrated copper vias with an aspect ratio of 10 (5µm diameter, 50µm deep).

Frederic Voiron, Senior R&D Engineer at IPDIA gave a good illustration of what 2.5D passives interposers could bring into the equation. Thanks to his company’s passive integration connecting substrate (PICS-IPD), hundreds of passive components could be integrated into a single silicon interposer, he said, claiming the world record of capacitance density in silicon, with 250nF/mm² in production (on 100 µm wafers) and 500nF/mm² tested and demonstrated. The technology could be combined with TSVs to build system-in-package solutions or even passive dies stacking for volume-constrained application.

Thorbjörn Ebefors, Chief Technologist, co-founder and VP of R&D at Silex Microsystems had a particular eye on TSVs for MEMS solutions. For MEMS applications, TSVs are used either through the sealing cap or through the bulk substrate and at much lower densities, typically 1 to 10 TSV/mm². They allow for compact MEMS-ASIC packaging, either wirebond or flip chip. The TSVs can be built directly into the MEMS substrate, eliminating the need for an organic substrate or interposer altogether (all-silicon package). Silex Microsystems offers two types of TSV technologies: the Sil-Via rigid interposer developed in 2003 across the full wafer thickness and a more recently developed Met-Via baseline process released in 2010, for TSVs through the MEMS cap. The ability to create TSVs through full wafer thickness means the interposer can be the package, using existing wafer processing, without exotic thin wafer handling. Again, the silicon substrate can be “functionalized” with passive or active elements. For example the MEMS cap wafer could integrate vertical capacitors, but also inductive coils with a magnetic core for driving the MEMS structures.



Nano-porous gold bumps for chip to substrate bonding by Fraunhofer- IZM / ASSID

IPDIA’s passive integration connecting substrate (PICS-IPD) with its embedded capacitors: concept and micrograph.

The latter can be realized as a combination of Met-Via TSVs and copper-traces on the wafer's surfaces with a layer of FeNiCo alloy trapped into the windings.

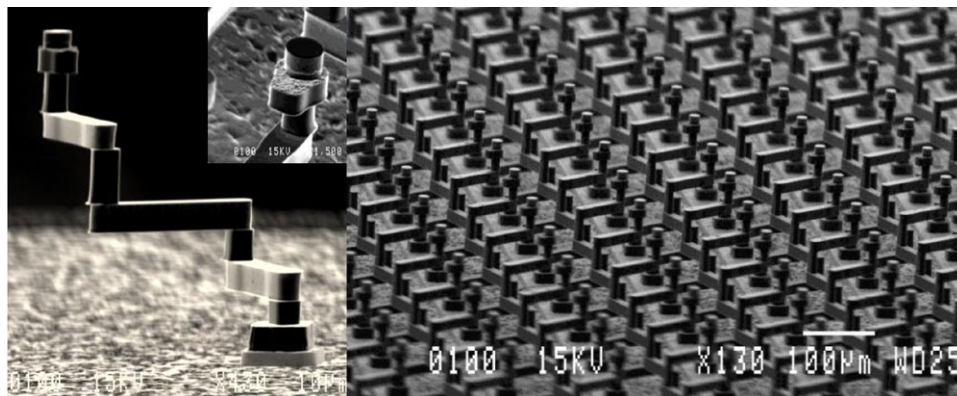
3D stack testing

Working with known-good-dies won't be enough to secure high 3D IC yields, and new testing strategies need to be developed.

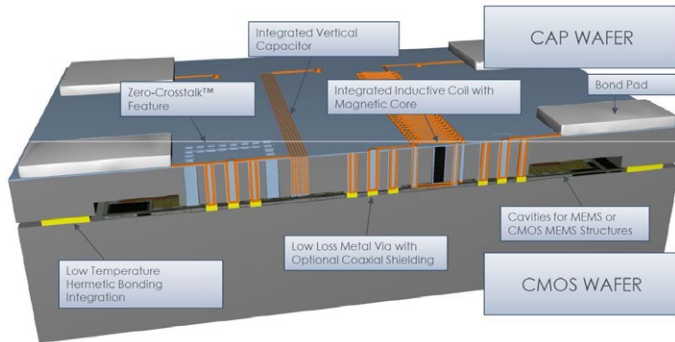
Design-for-test is the way to go, was the main message from Brandon Wang, Director 3D IC and Advanced Technology Product Management at Cadence Design System. First you need the tools for design partitioning, at different technology node for each die, then you must look at the die orientation and stacking orders, and last you must analyse performance (delay, latency), power distribution (thermal issues) and mechanical stress. This calls for a co-design between the package, the IC stack and the interposer for optimized TSV and bump locations, cross die bump optimization and best power plans. This is when you must design the interconnects and die-internal circuitry to ensure test access at the bottom die, in a way that allows test stimuli and response propagation up and down through the final 3D stack. This systematic approach requires new layout rules. In collaboration with imec, the EDA company has implemented and validated an automated 3D Design-for-Test (DFT) solution to test logic-memory interconnects in DRAM-on-logic stacks. Based on Cadence Encounter Test technology, the solution was verified on an industrial test chip containing a logic die and a JEDEC-compliant Wide-I/O Mobile DRAM (on an interposer). The solution supports post-bond testing of the interconnects between the logic die and the DRAM stacked on top of it. It also includes the generation of DRAM test control signals in the logic die and the inclusion of the DRAM boundary scan registers in the serial and parallel test access mechanisms (TAMs) of the 3D test architecture. The inserted 3D DFT wrapper IP had a negligible impact on die area, at about 0.3% of total circuit silicon footprint. Wang also disclosed a thermal analysis flow and an IR drop analysis flow where all the micro-bumps and TSVs are modelled as RC or RLC networks while all the chips are analysed at the same time for accurate results.

So what about accessing these tiny test pads at the bottom of the stack?

Senior Director for Business Development at Advantest, Gary Fleeman hinted at MEMS-based micro-probe tips that would not break the thin wafers nor dig marks on the copper traces. Advantest is evaluating the InfinityQuad probe technology developed by Cascade Microtech, with monolithically fabricated tips at a 40 µm pitch, with a positional accuracy to within 1 µm and excellent planarity (a prerequisite for good contact yield). Another MEMS-based approach under development from sister company TouchDown Technologies relies on a swinging probe tip that would yield lower tip forces (under 1 gram-force) for a lesser pad damage. In principle, such approaches would be scalable to finer pitches.



New MEMS-based micro-probe tips from TouchDown Technologies could rely on a swinging probe tip to yield lower tip forces for a lesser pad damage.



Silex' MEMS cap wafer could integrate vertical capacitors, but also inductive coils with a magnetic core for driving the MEMS.

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Sensor interface IC facilitates implementation of gesture recognition applications

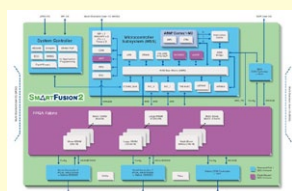
The MLX75030 from Melexis is a universal active light sensor interface designed to allow easy implementation of robust multi-channel, close range optical sensing systems into difficult operational environments. The MLX75030 incorporates four independent simultaneously operating light measurement channels; two taking care of reflection and the other two for ambient light measurement. The Melexis chip features two active light reflection measurement channels with integrated ambient light suppression. The active light sensing section is complemented by two logarithmic current sensors which can measure the photocurrent signal from externally connected photodiodes for ambient light sensing. Internal control logic, configurable user registers and SPI communication enable simple, programmable operation. The optical light intensity of both active light channels can be used to detect proximity of an object close to the detectors, independent from the background light level. Human gestures (such as swipes or zooms) can then be determined by use of software algorithms. HMI response times of 30 frames/sec are supported. The MLX75030 is offered in a 4x4mm, 24-pin surface mount QFN package, or as a bare die. Versions supporting both standard 0°C to 70°C and extended -40°C to 105°C operational temperature ranges are available.

Melexis

www.melexis.com

SmartFusion starter kit with breadboard and smartphone access

Microsemi has launched a Starter Kit for its SmartFusion 2 FPGA, providing designers with a basic prototyping platform that includes a breadboard area for custom interfaces. Acces-



sible via a smartphone, the Kit supports industry-standard interfaces including Ethernet, USB, SPI, I²C and UART and includes a comprehensive breadboard to support unique design requirements. The kit can be used with

Microsemi's Libero SoC v11.0 beta software, which includes a free Libero Gold license and comes preloaded with a uClinux demo. By using the included USB WiFi adapter, the kit has support for RaLink 5370 USB wireless radios, allowing uClinux to setup a wireless access point that serves DHCP WiFi connections. Users can start a HTTPD server and then access the SmartFusion2 device via a smart phone web browser or other wireless device. Emcraft Systems' Linux-based development environment is also supported. The SmartFusion2 device is available on an Emcraft Systems miniature (34x59mm) mezzanine form factor system-on-module (M2S-SOM), which connects to the SOM-BSB-EXT baseboard. The kit is USB powered, includes FlashPro4 programming and features the SmartFusion2 SoC FPGA in the FG896 package (M2S050T-FG896ES) with a USB based Wi-Fi module, 64MB of LPDDR system memory and 16MB of SPI flash memory.

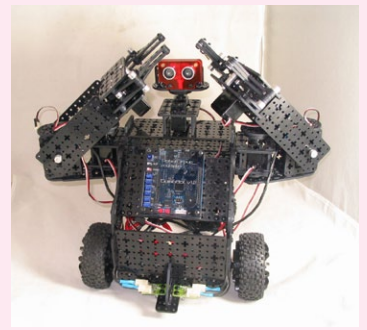
Microsemi

www.microsemi.com

Three robot building kits to win: make your own robots



This month, Multiplo is giving away three Robot Building Kits, worth USD 239 each, for EETimes Europe's readers to win. The 'N8 Robot kit' developed by Multiplo, is a low-cost, Arduino software and open hardware kit with plenty of documentation and all the pieces needed to design and prototype your own fully-functional robots. Beginners with no experience can follow the tutorials and examples while more experienced users can create their own designs. Users can program with Arduino software but unexperienced programmers can also try with Minibloq, a really intuitive graphical programming environment that is fully compatible with Arduino. Multiplo is based on a mathematical model that keeps each part compatible with the others. The basic principle is that all parts can be reproduced with simple tools. All C.A.D. files are available in a public repository for advanced users to design their own parts. All boards and sensors that come with the N8 Robot kit are simple to configure, their datasheets and blueprints can be downloaded and edited (under open source based license).

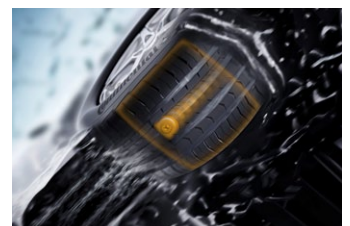


Check the reader offer online at

www.electronics-eetimes.com

Tire sensors detect vehicle weight

Automotive supplier Continental will expand the scope of its tire pressure sensors. Continental is currently developing a generation of pressure sensors that are smart enough to determine the total weight of the vehicle. For the automatic load detection system, the engineers take advantage of the physical properties of vehicle tires. The contact patch of the tire increases as a result of the weight bearing down on the tire. With the future generation of sensors, which will be fitted directly underneath the tread of the tire, the tire pressure monitoring system can accurately detect the size of this contact area. With the revolutions of the wheel, the associated pressure sensor registers the rolling characteristics of the tire on the road. Based on the existing tire pressure and precise data about characteristics of the tires fitted, the system is able to inform the driver after just a few hundred meters if a change in tire pressure would be appropriate for the current payload. This kind of load detection also can be used as the basis for new assistance systems. Systems such as Electronic Stability Control, Emergency Steer Assist or Autonomous Emergency Braking Assistant can take the actual vehicle weight into account and thus achieve better results.

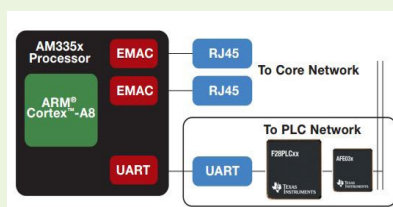


Continental

www.conti-online.com

Smart data concentrator module cuts nine months from developments

Texas Instruments has launched a Smart Data Concentrator Evaluation Module (EVM) that can cut months from the development of a smart meter design. The TMDSDC-EV-



MAM335x is a highly integrated EVM based on TI's Sitara AM335x ARM Cortex-A8 processors with advanced hardware and software that reduce development time

by up to nine months while still supporting connectivity to more than 1,000 smart meters. The Smart Data Concentrator EVM expands the functionality of designs and enables quick connectivity to the smart grid. Developers can easily plug in different connectivity modules, including Sub-1GHz (LPRF), general packet radio service (GPRS), near field communication (NFC) and TI's power line communication (PLC) system-on-module contains a C2000 Piccolo F28PLC83 and AFE031 analog front end for robust G3 and PRIME support. In addition, the data concentrator EVM offers an extensive open-source Linux software development kit that includes fully customizable, pre-written code. Developers can easily add functionality and features to data concentrator designs without the hassle of writing and tweaking code. It also includes resources such as PLC stacks (PLC-Lite, PRIME, G3, IEEE-P1901.2), network protocols and applications like DLMS/COSEM so developers can customize their products for multiple regional and global standards.

Texas Instruments
www.ti.com

Compact dual mode Wi-Fi network controller targets home appliances

Murata's SN8200 series of compact low power certified Wi-Fi controller modules are capable of providing 2.4GHz 802.11b/g/n internet connectivity to a broad host of home appliances, industrial automation machines and healthcare equipment. The self-contained module uses Broadcom Corporation's wireless internet connectivity for embedded devices (WICED) architecture to provide comprehensive firmware and software features including a built-in Wi-Fi security supplicant supporting WPA PSK and WPA2 PSK, TCP/IP network stack and a simple network interface card (SNIC) protocol that supports socket connections. Measuring just 30.5x19.4x2.9mm, the SN8200 module is certified to FCC, IC and ETSI wireless standards and is equipped with a STM32 ARM Cortex-M3, an on-board antenna and offers both UART or SPI connectivity to the host application. The ability to support sensor applications is also possible by using the module's ADC, DAC, I2C and GPIO interfaces. The SN8200 can operate in either access point (AP) or station (STA) mode. An integrated web server available in AP mode makes target device setup and control extremely easy. Output power is typically +18 dBm when operating in 802.11b mode at 11 Mbps.



Murata Europe
www.murata.eu

Pin-in-Paste RF MoCA filter modules withstand a reflow temperature of 260°C

Pulse Electronics has introduced RF MoCA (Multimedia over Cable Alliance) filter modules that are pin-in-paste compatible. Pin-in-paste manufacturing uses a reflow instead of a



wave soldering process to apply solder to the components, saving time, increasing throughput, and reducing costs. These filters are compliant with MoCA 1.1 and 2.0 requirements and are qualified with leading MoCA silicon vendors. A fil-

ter module can be configured as a multiband diplexer /triplexer with CATV (Cable TV), satellite, and DOCSIS (Data Over Cable Service Interface Specification) frequencies with an optional built-in surge protection. They can withstand a maximum reflow temperature of 260°C and operate over an extended temperature range of -40° to +85°C. The pin-in-paste method (also called pin-in-hole, intrusive reflow, or through-hole reflow technology) is a process that allows through-hole components to be reflow-soldered instead of wave or hand soldered. Using solder reflow eliminates the cost of wave soldering equipment, saves manufacturing floor space, is a no-clean soldering process, reduces heat stress at the component level, is compatible with existing processes, and results in higher reliability at the printed circuit board level due to fewer soldering processes. The RF filters can also be inserted into the PCB using industry standard pick-and-place equipment. They are 100% tested.

Pulse Electronics
www.pulseelectronics.com

Digital solid-state LED driver platform enables cost efficient solutions

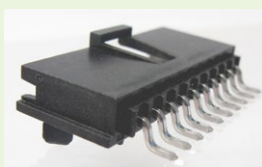
Chipmaker iWatt has launched a digital AC/DC solid state lighting (SSL) LED driver platform designed specifically to address the key issues of cost and lifetime in price-sensitive, non-dimmable, residential SSL bulb applications. The first device in this new platform is the iW3626, a single-stage driver with output power up to 10W for 60W-equivalent, non-dimmable LED bulbs. According to iWatt, the iW3626 allows SSL designers to reduce their bill of materials (BOM) cost as much as 20% compared to competitive solutions and is believed to be the first SSL LED driver to offer an on-chip, user-configurable power factor correction (PFC) to manage the trade-off between PFC and output current ripple. Additionally, an internal, configurable over-temperature protection (OTP) and derating function enables a predictable and reliable bulb operating life. This combination of features gives LED bulb manufacturers new options for lower-cost, higher-performance, non-dimmable SSL incandescent bulb replacement applications. The user-configurable PFC feature in the iW3626 allows designers to configure the PF strength from > 0.7 to > 0.9, enabling them to meet the various global mandates while effectively managing the trade-off between power factor and output ripple. The iW3626 is packaged in a standard, low-cost, 6-lead SOT23 package.



iWatt
www.iwatt.com

Male 90° SMT connectors with latch and PCB pegs

Nicomatic has released latched male 90° SMT headers with latch and molded pegs which align and brace the PCB tails for trouble free assembly and use. These new headers are



designed to enable 90° soldering on PCB. Two functions allow the right PCB integration thanks to PCB pegs made for plated or non-plated holes: a perfect placement on PCB and excellent PCB

retention. Whilst the PCB pegs is usually sold as an option, Nicomatic has considered it as a standard product for the SMT 90° PCB integration of the header (solder process). The triangular shape of the pegs allows headers to hold well on PCBs. Even without soldering, if the engineer needs to check the component placement, he or she can take the PCB upside down without losing it. The new headers are available under P/Ns 1L-10-5Y1-XX-1-P (XX = from 02 to 20 ways) set in a variety of single row configurations with a 2.54mm pitch. The product is also 100% compatible with 2.54mm pitch Crimpflex female housings OL(H)xx, OM(H)xx and OJ(H)xx & 2SL discrete wire housings. It is manufactured of Glass filled plastic with a flammability rating of UL94V-0. In the standard series, contacts can be selected tin-plated, selectively gold-plated or fully gold-plated. Contact resistance is 20mΩ maximum with 3A of current rating per contact. Mechanical endurance is 500 operations with gold contacts.

Nicomatic
www.nicomatic.fr

Configurable CAD models for Brushless DC motors

Pittman Motors has introduced configurable 3D CAD model downloads for its entire offering of brushless DC motors. The 3D model system is an online system through the company's website that allows an engineer to fully configure a motor with a wide variety of optional components, such as planetary and spur gearboxes, brakes, and encoders. The online 3D model system makes it very easy for an engineer to evaluate different part configurations in a virtual environment. A customer can configure a part by choosing such parameters as motor voltage, torque rating, gearbox ratio, and encoder resolution. After configuring a part as many times as necessary, the file can then be downloaded in the most commonly used CAD software file formats including Solid Works, CATIA, and Pro/E. The file also can be downloaded in a vendor-neutral format, such as an .IGS or .STP file. The system allows the creation of a fully dimensioned outline drawing generated directly from the configured CAD model. After a virtual configuration is created using the online 3D model system, a product engineer can work closely with Pittman applications engineers to create a more customized application-specific solution. Options include optimized motor windings, unique shaft configurations, various bearing systems, output devices such as pinions and pulleys, special lead wire assemblies, and various other features.

Pittman Motors
www.Pittman-Motors.com



Network LED dimmer controls LED brightness over serial networks

Industrial automation manufacturer Opto 22 has announced the Network LED Dimmer, a compact, solid-state, and networkable LED dimmer that uses pulse width modulation (PWM) to control LED brightness (0-100%) for 9-30 VDC constant voltage LED lighting assemblies such as lamps, bulbs, strips, ropes, and bars.

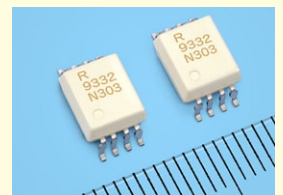
Used alone or teamed with other Dimmers, the Network LED Dimmer is suitable for any application that requires variable light from LEDs. Lighting designers, facility engineers, and architects can use the Dimmer in applications such as stage or accent lighting, LED color mixing, path marking, backlighting, and facade or wall lighting. When connected to an RS-485 serial network, multiple Network LED Dimmers can be integrated into a lighting, automation, or building control system that supports DMX512-A, Modbus/ASCII, or Optomux network protocols. The compact Network LED Dimmer is also suited for vehicle and vessel applications, where energy efficiency and long life of low-voltage LED lighting is critical. The Dimmer includes a built-in test pushbutton for ramping LED intensity up and down, connectors for wiring a pushbutton for manual operation, and indicator lights to show serial communication and ramping operation. As with other Opto 22 products, the Network LED Dimmer has a QR code imprinted on the inside cover that makes current documentation and configuration information available immediately.



Opto 22
www.opto22.com

Photocouplers offer high-speed switching and integrated IGBT protection function

Renesas Electronics has introduced two new photocouplers PS9332L and PS9332L2, with an integrated insulated-gate bipolar transistor (IGBT) protection function, for applications such as industrial machinery and solar power systems. The new PS9332L and PS9332L2 feature an integrated active Miller clamp circuit to prevent IGBT malfunction, world-top-class high-speed switching (20 percent faster than conventional products) among IGBT drive photocouplers with integrated IGBT protection function, compact 8-pin SDIP (shrink dual inline package), and guaranteed high-temperature operation. The photocouplers can be used for gate drive of IGBT devices used in inverter circuits for motor control. A photocoupler combines in a single package a light emitting diode (LED) on the input side, to convert an electrical signal into light, and a photo detector on the output side, to convert the light into an electrical signal. The input and output sides are electrically isolated from each other because the signal is conveyed between them in the form of light. Types of photocouplers include general-purpose photocouplers (transistor output) for applications such as power supply, and IGBT drive photocouplers, which are used for gate drive of IGBT devices in applications such as solar power generators or general-purpose inverters.



Renesas Electronics Europe
www.renesas.eu

Mouser signs worldwide distribution agreement with Altera for programmable logic

Mouser Electronics, Inc., signs a worldwide distribution agreement with Altera Corporation which will see Mouser become an authorized global distributor of Altera FPGAs, CPLDs, development tools, intellectual property cores and development kits. Mouser gives design engineers fast, easy access to the widest range of semiconductor technologies. Mouser's distribution agreement with Altera boosts the Mouser catalog of products and expands the availability of leading-edge programmable solutions from Altera to designers around the world. Mouser will distribute Altera's full range of products to customers in a variety of end markets, including communications, broadcast, automotive, industrial, compute and storage, test and measurement, military and medical. Mouser's Web site will also provide design engineers easy online access to Altera technical documentation for ease-of-design and increased productivity.

Mouser Electronics, Inc.
www.mouser.com/altera/

Rapid Electronics delivers Winstar's E-paper modules

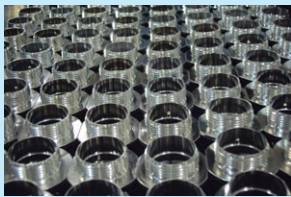
Anyone who has read an e-book will know how impressive the digital reading experience is. This is made possible by E-Paper technology – electrophoretic display modules. A range of new Winstar E-Paper modules, with 6 and 10 segment variations are now available from Rapid Electronics. Electrophoretic display modules (EPD) operate through reflected rather than emitted light, designed to mimic the appearance of ordinary ink on paper. Flexible, durable and impact resistant, these Winstar modules have an extremely long lifetime, with the ability to be updated up to 1 million times. Featuring high whiteness, high contrast ratio and bi-stability, the modules do not need power to retain an image.



Rapid Electronics
www.rapidonline.com/e-paper

Arrow Electronics launches EMEA connector assembly facility

Arrow Electronics has opened a new connector assembly facility for its component customers in EMEA. Situated in Venlo, Netherlands, the operation will support companies

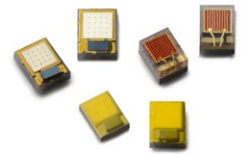


in the aerospace, defence and industrial sectors with made-to-order connectors and assemblies. The facility is qualified to ISO9001:2008, ISO 14001:2004 and IECQ-CECC and can support standardized and customized configurations. Special handling, packaging, labelling, bar coding, kitting and control documentation is also available.

Arrow Electronics
www.arroweurope.com

Avnet Abacus supports SILICA agreement with Philips Lumileds for lighting solutions

Avnet Abacus has started stocking a comprehensive range of power, interconnect, thermal management, device control and protection components designed specifically for solid-state lighting applications. The products complement and support the LED lighting portfolio of SILICA, another business unit of Avnet Electronics Marketing, which announced a pan-European franchise agreement with Philips Lumileds, a leading manufacturer of high-power LEDs. With the combined product portfolios of Avnet Abacus and SILICA, customers have access to a complete range of components for their solid-state lighting applications.



Avnet Abacus
www.avnet-abacus.eu

Distec offers customized TFT display shapes and sizes for digital signage

German specialist for TFT-LCD flat screens and systems, Distec broadens its product platform with digital signage solutions in new and unique formats. Customized width-to-height ratios are



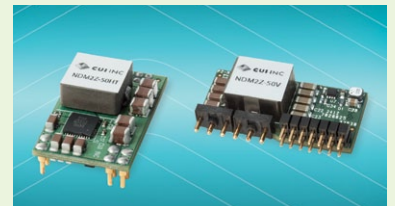
now possible with horizontal and vertical alignment. The company now offers triangles and other eye-catching formats for point-of-sales usage. It can accommodate small format requests. Additional applications for ultra-widescreen displays include way-finding for public

transportation or shopping areas and menu boards for fast food and quick service restaurants (QSR). Any TFT display with a removable frame and mechanism can be customized but edge LED backlight is favoured. The laser technology cuts and seals the LCD coating in one simple step, allowing for pixel-perfect cuts with no degradation of image quality.

Distec
www.distec.de

CUI and Future Electronics sign global distribution agreement

CUI Inc, a subsidiary of CUI Global, has signed a global distribution agreement with Future Electronics, enabling the distributor to begin a phased rollout of products from CUI's Power and Components groups with stock available immediately for many items. "We are very pleased to be launching the CUI franchise," said Jodie Metsos, Vice President of Corporate Product Marketing for Future Electronics. "Their line of Power Supplies and board level components has had a tremendous amount of interest from our sales and engineering teams and most importantly, our customers. We see a very positive outlook for the Future/CUI partnership."



Future Electronics
www.FutureElectronics.com

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LAST WORD

Bench-top cleaning: Be careful what you ask for

By Mike Jones

BENCH-TOP CLEANING is superficially very simple, yet it is a challenging industrial process. This is because the requirements for successful bench-top cleaning are very different than the requirements for a chemical to be used in an automated cleaning machine.

A cleaning fluid must meet a number of criteria to make it an acceptable product for workers to use on the bench-top. It must have exceptionally good toxicity profiles and should be fast drying and with no aroma, and preferably with no flashpoint. The cleaner has to be easy to use, handle, store, dispose of and affordably priced. It must also be powerful, but not so strong as to attack substrates and components being cleaned.

There are not many chemicals that can meet all of these criteria. On top of these performance requirements are new regulations being imposed around the world, inconsistently and often by regulators with little knowledge or interest in the particular problems of employees working on the bench-top or the companies that pay them. REACH in the EU, and the new CLP rules in Europe limit the choices engineers make. These dynamic regulatory pressures are eliminating many otherwise promising chemistries.

Another constraint is the current packaging and labeling requirements. Many countries now require safety labeling in local languages, which is a worthy goal. But there are 23 official languages in the EU. The unintended effect of this requirement is to push companies out of smaller markets, denying customers in those regions the benefits of innovative chemical technologies simply because it is not possible to get safety warnings in 23 languages on a label. Lastly, many

regulatory decisions are made without considering the entire workflow. For example, in many locations the recommended cleaning fluid is water because it is deemed as 'green' and 'environmentally safe'. This is an over-simplification, as water does not work in every application such as in bench-top de-fluxing.

Furthermore, since burning fossil fuels to produce electricity is one of the main sources of greenhouse gasses, any migration to water-based cleaning will have the unintended and undesired effect of increasing greenhouse gas emissions. Like it or not, increasing regulatory pressures are a fact of life and companies are going to have to adapt to them.

Better choices require new

guidelines

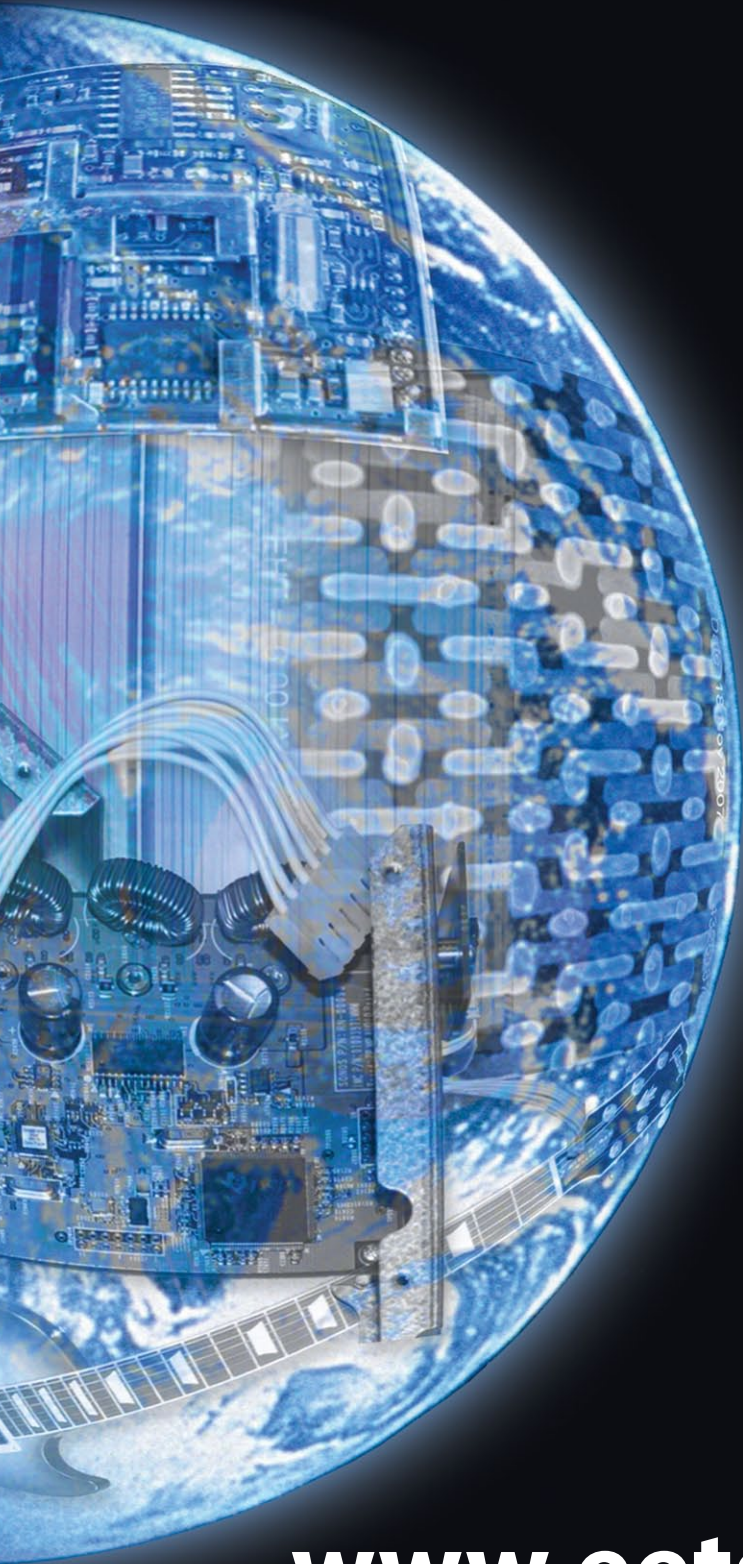
For busy manufacturing engineers, finding, evaluating and approving bench-top de-fluxers and cleaners is a time-consuming and expensive process. A few simple rules may help simplify the selection process:

1. Any alternative chemical selection should limit consideration only to commercially available materials that have long-term market viability. Materials subject to international regulatory scrutiny that could affect long-term availability should be avoided.
2. Engineers must consider not just the chemical itself but the packaging in which it comes. Modern packaging can enhance the effectiveness of a cleaning fluid as well as minimize any environmental impact and improve worker safety. To make a solvent selection by simply comparing MSDS sheets, for example, is to miss a big part of the cleaning story.
3. Finally, engineers need to consider the cleaning process itself. The old-style 'dip-and-brush' cleaning is obsolete. Several manufacturers now provide cleaning tools designed to work and enhance their cleaning fluids. These tools can dramatically improve cleaning performance whilst reducing cleaning costs.



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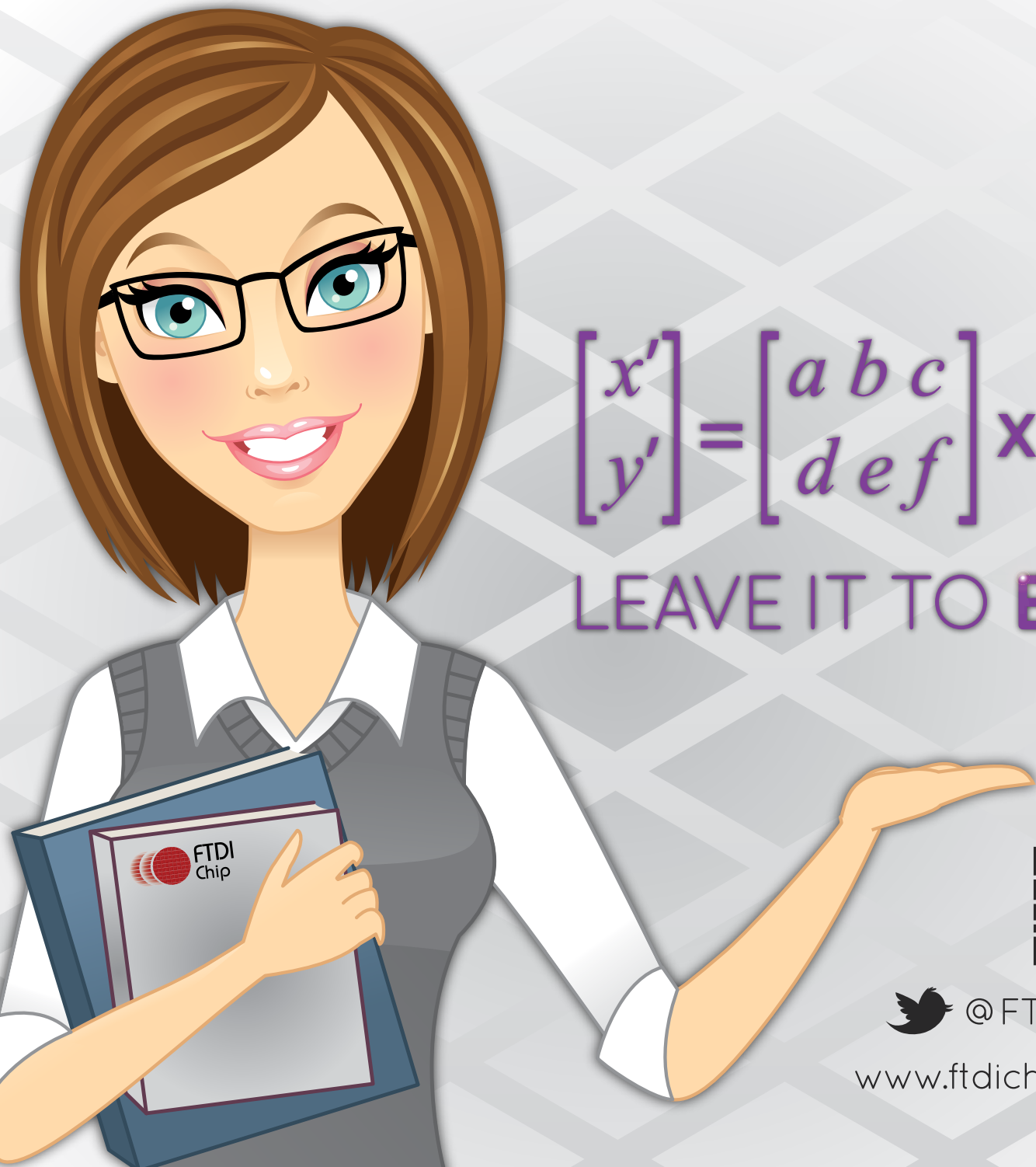
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